Semiconductor Fabrication Process

(반도체공정개론)

장소: 공과대학 6호관 510호

시간: 화 (1-A, 1-B, 2-A, 2-B, 3-A, 3-B)

Objectives

Overview of Silicon Technology

- Wafer preparation
- Lithography
- Oxidation
- Etching
- Doping
- Deposition
- Packaging

Common Dopants Used in Semiconductor Manufacturing

Acceptor Dopant Group IIIA (P-Type)		Semiconductor Group IVA		Donor Dopant Group VA (N-Type)	
Element	**Atomic Number**	**Element**	**Atomic Number**	**Element**	**Atomic Number**
Boron (B)	**5**	Carbon	6	Nitrogen	7
Aluminum	13	Silicon (Si)	14	**Phosphorus (P)**	**15**
Gallium	31	Germanium	32	**Arsenic (As)**	**33**
Indium	49	Tin	50	**Antimony**	**51**

CMOS Structure with Doped Regions

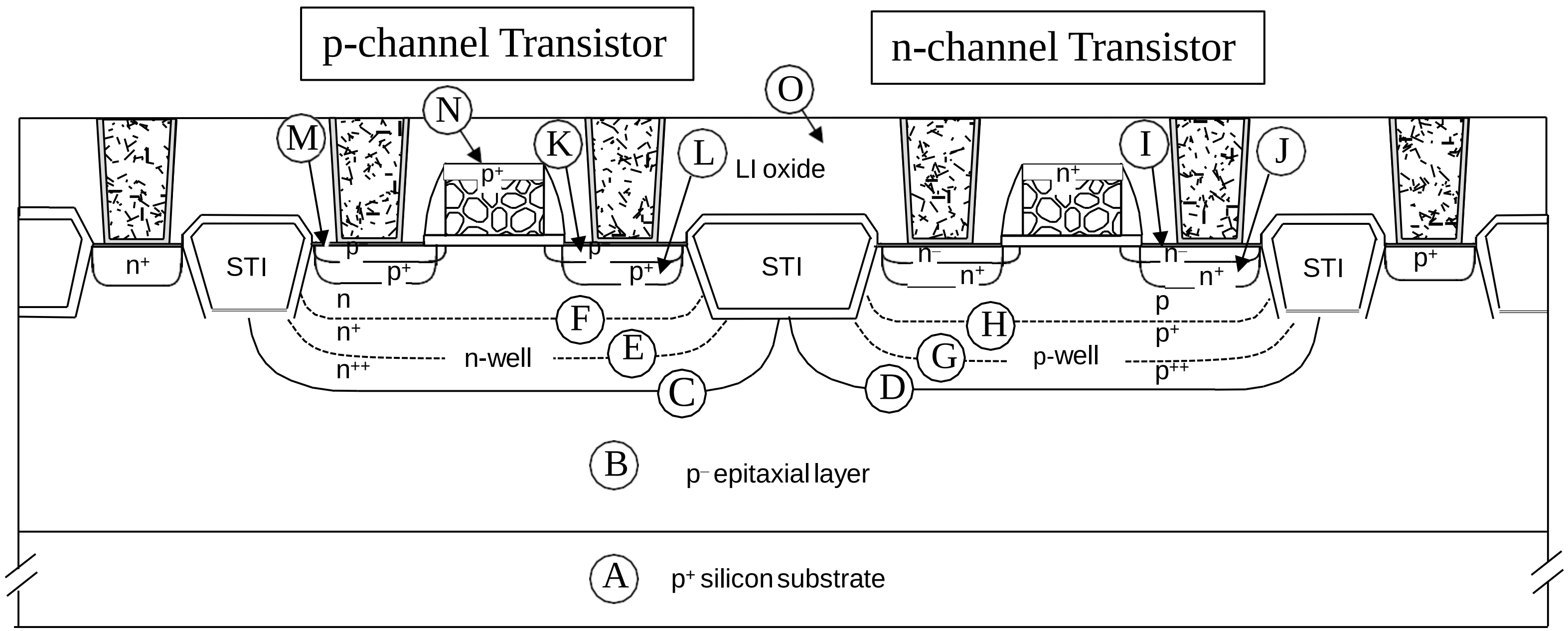
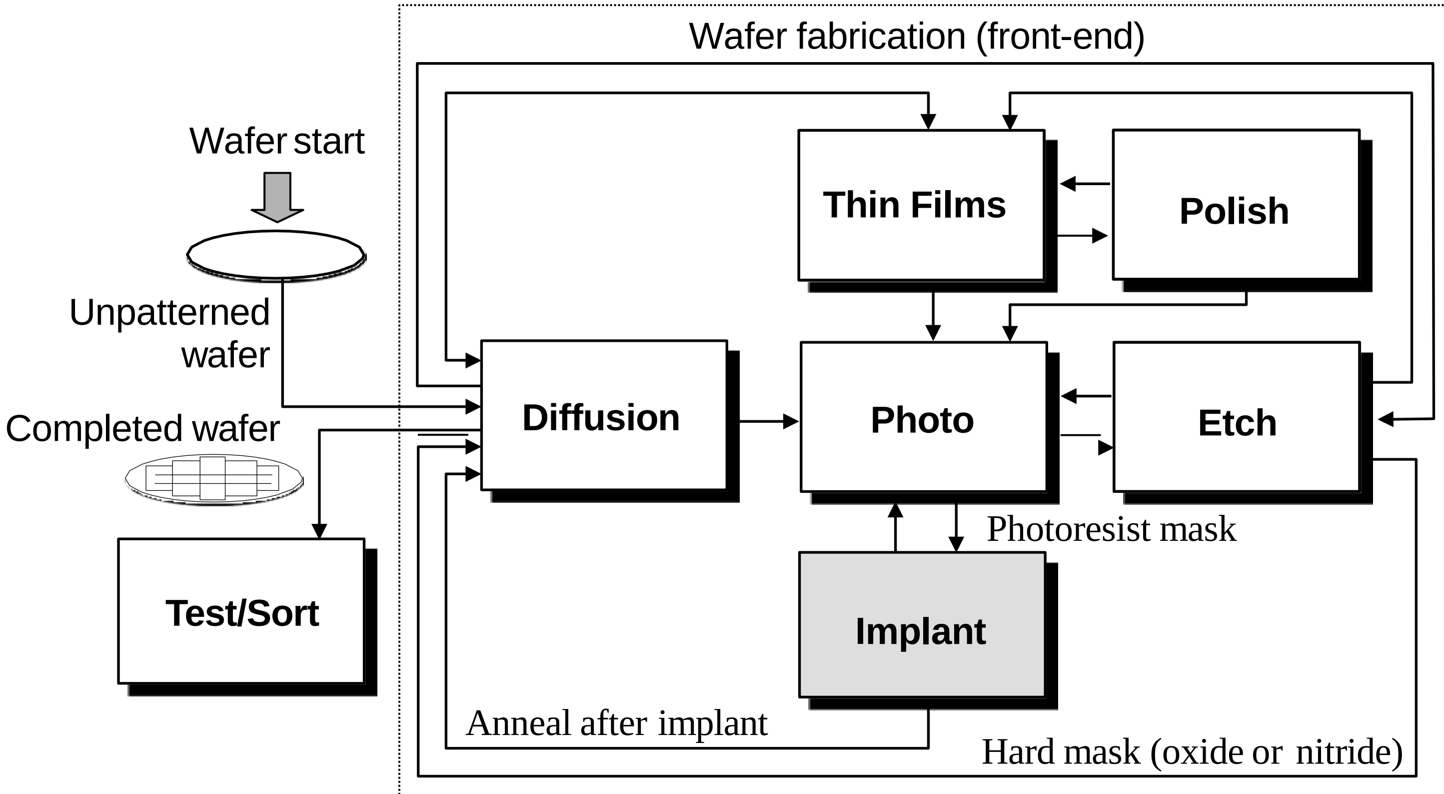


Figure 17.1

Common Dopant Processes in CMOS Fabrication

Process Step	Dopant	Method
A. p+ Silicon Substrate	B	Diffusion
B. p^- Epitaxial Layer	B	Diffusion
C. Retrograde n-Well	P	Ion Implant
D. Retrograde p-well	B	Ion Implant
E. p-Channel Punchthrough	P	Ion Implant
F. p-Channel Threshold Voltage (V_T) Adjust	P	Ion Implant
G. p-Channel Punchthrough	B	Ion Implant
H. p-Channel V_T Adjust	B	Ion Implant
I. n-Channel Lightly Doped Drain (LDD)	As	Ion Implant
J. n-Channel Source/Drain (S/D)	As	Ion Implant
K. p-Channel LDD	BF_2	Ion Implant
L. p-Channel S/D	BF_2	Ion Implant
M. Silicon	Si	Ion Implant
N. Doped Polysilicon	P or B	Ion Implant or Diffusion
O. Doped SiO_2	P or B	Ion Implant or Diffusion

Ion Implant in Process Flow



Used with permission from Lance Kinney, AMD

Doped Region in a Silicon Wafer

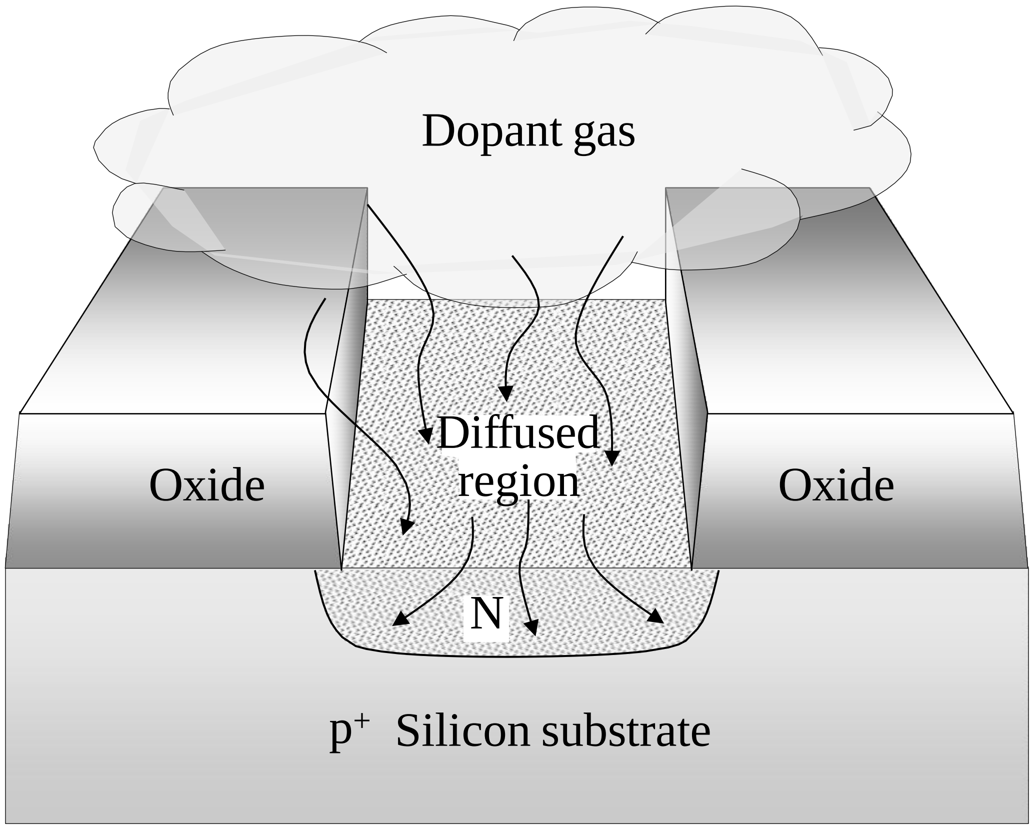
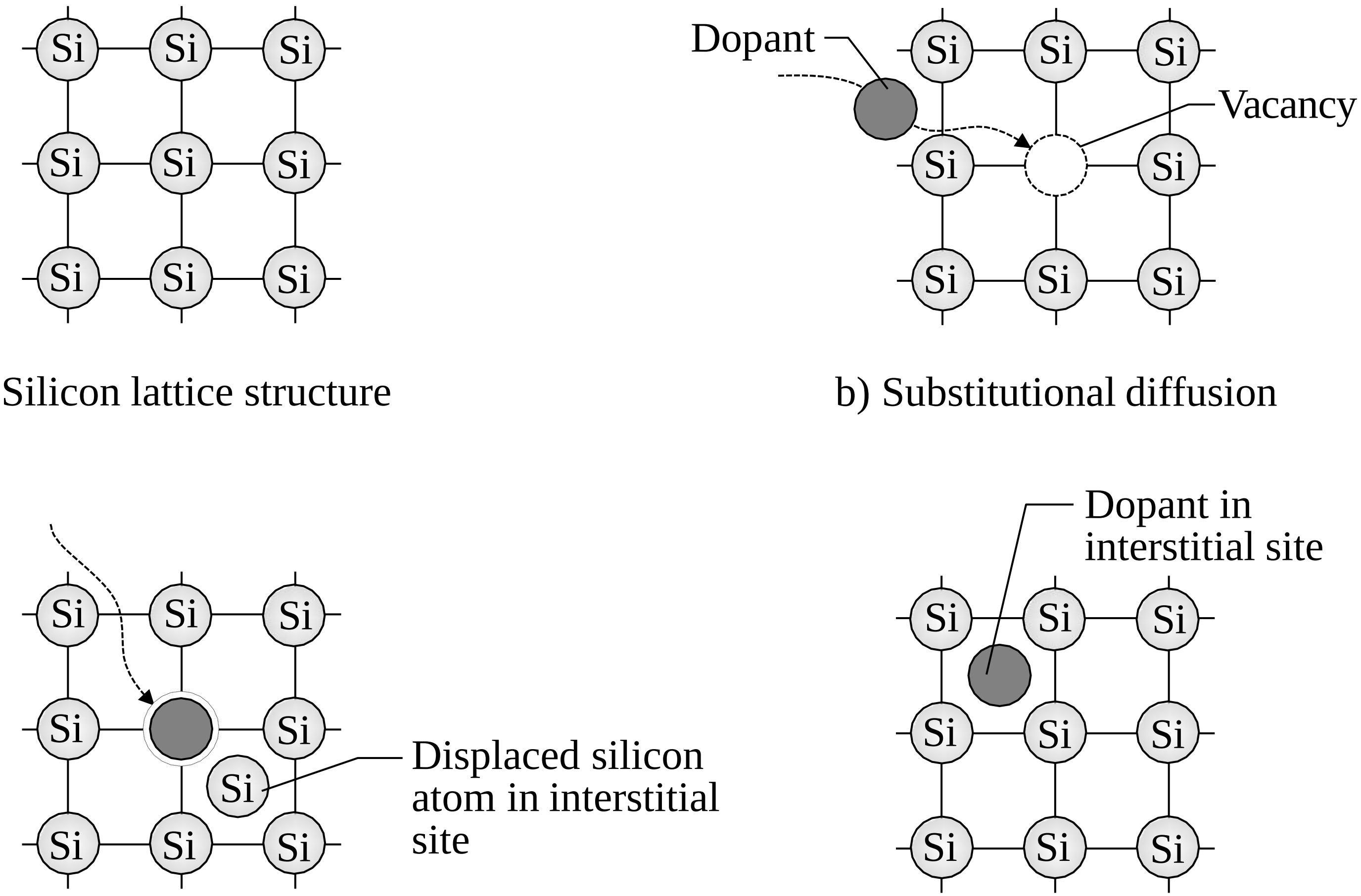


Figure 17.3

Diffusion

- Diffusion Principles
  - Three Steps
    - Predeposition
    - Drive-in
    - Activation
  - Dopant Movement
  - Solid Solubility
  - Lateral Diffusion
- Diffusion Process
  - Wafer Cleaning
  - Dopant Sources

Dopant Diffusion in Silicon



a) Silicon lattice structure

b) Substitutional diffusion

c) Mechanical interstitial displacement

d) Interstitial diffusion

Figure 17.4

Solid Solubility Limits in Silicon at 1100˚C

Dopant	Solubility Limit (atoms/cm^3)
Arsenic (As)	1.7×10^{21}
Phosphorus (P)	1.1×10^{21}
Boron (B)	2.2×10^{20}
Antimony (Sb)	5.0×10^{19}
Aluminum (Al)	1.8×10^{19}

Table 17.3

Diffusion Process

Eight Steps for Successful Diffusion:

1. Run qualification test to ensure the tool meets production quality criteria.
2. Verify wafer properties with a lot control system.
3. Download the process recipe with the desired diffusion parameters.
4. Set up the furnace, including a temperature profile.
5. Clean the wafers and dip in HF to remove native oxide.
6. Perform predeposition: load wafers into the deposition furnace and diffuse the dopant.
7. Perform drive-in: increase furnace temperature to drive-in and activate the dopant bonds, then unload the wafers.
8. Measure, evaluate and record junction depth and sheet resistivity.

Typical Dopant Sources for Diffusion

Dopant	Formula of Source	Chemical Name
Arsenic (As)	AsH_3	Arsine (gas)
Phosphorus (P)	PH_3	Phosphine (gas)
Phosphorus (P)	$POCl_3$	Phosphorus oxychloride (liquid)
Boron (B)	B_2H_6	Diborane (gas)
Boron (B)	BF_3	Boron tri-fluoride (gas)
Boron (B)	BBr_3	Boron tri-bromide (liquid)
Antimony (Sb)	$SbCl_5$	Antimony pentachloride (solid)

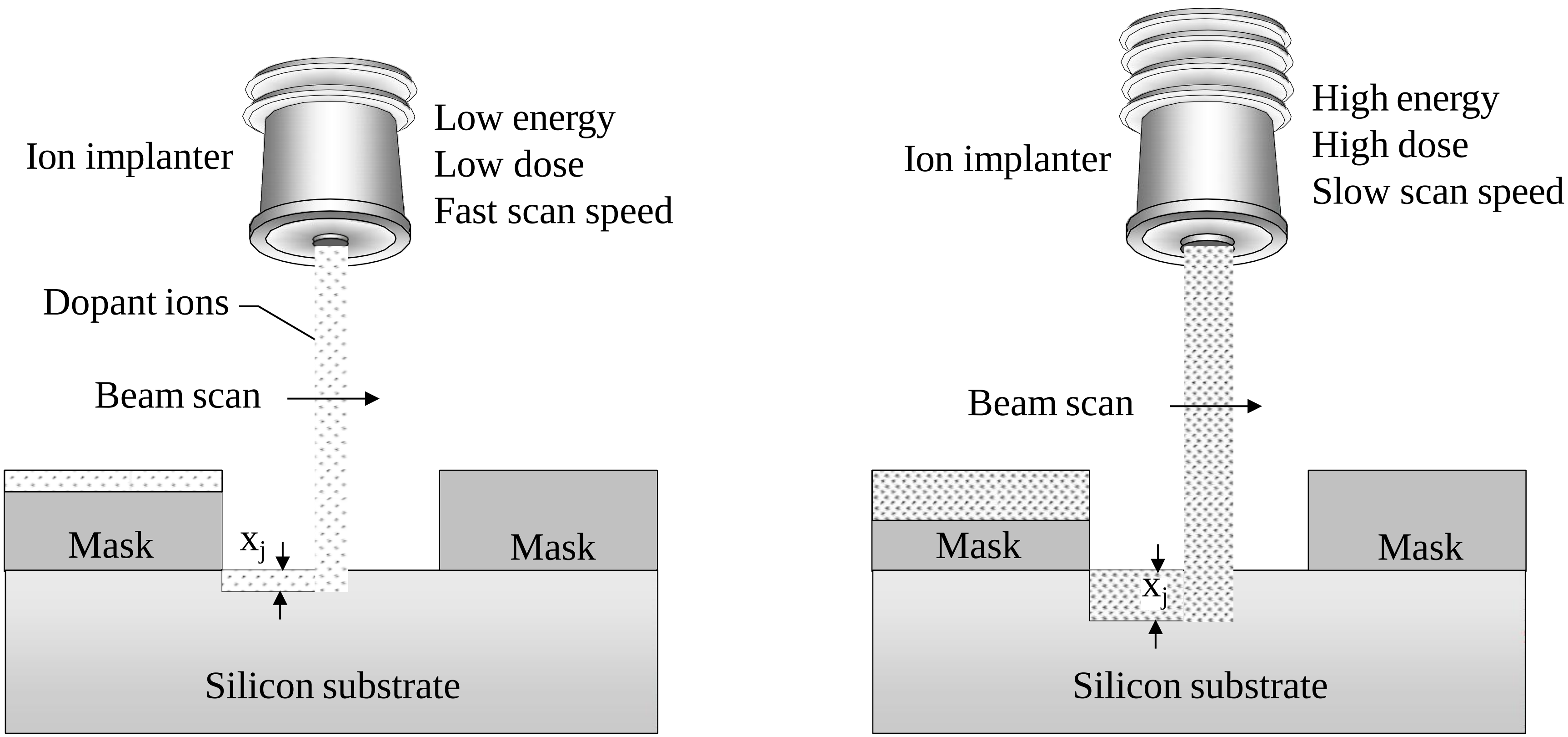
SEMATECH "Diffusion Processes," *Furnace Processes and Related Topics*, (Austin, TX: SEMATECH, 1994), P. 7.

Table 17.4

Ion Implantation

- Overview
  - Controlling Dopant Concentration
  - Advantages of Ion Implant
  - Disadvantages of Ion Implant
- Ion Implant Parameters
  - Dose
  - Range

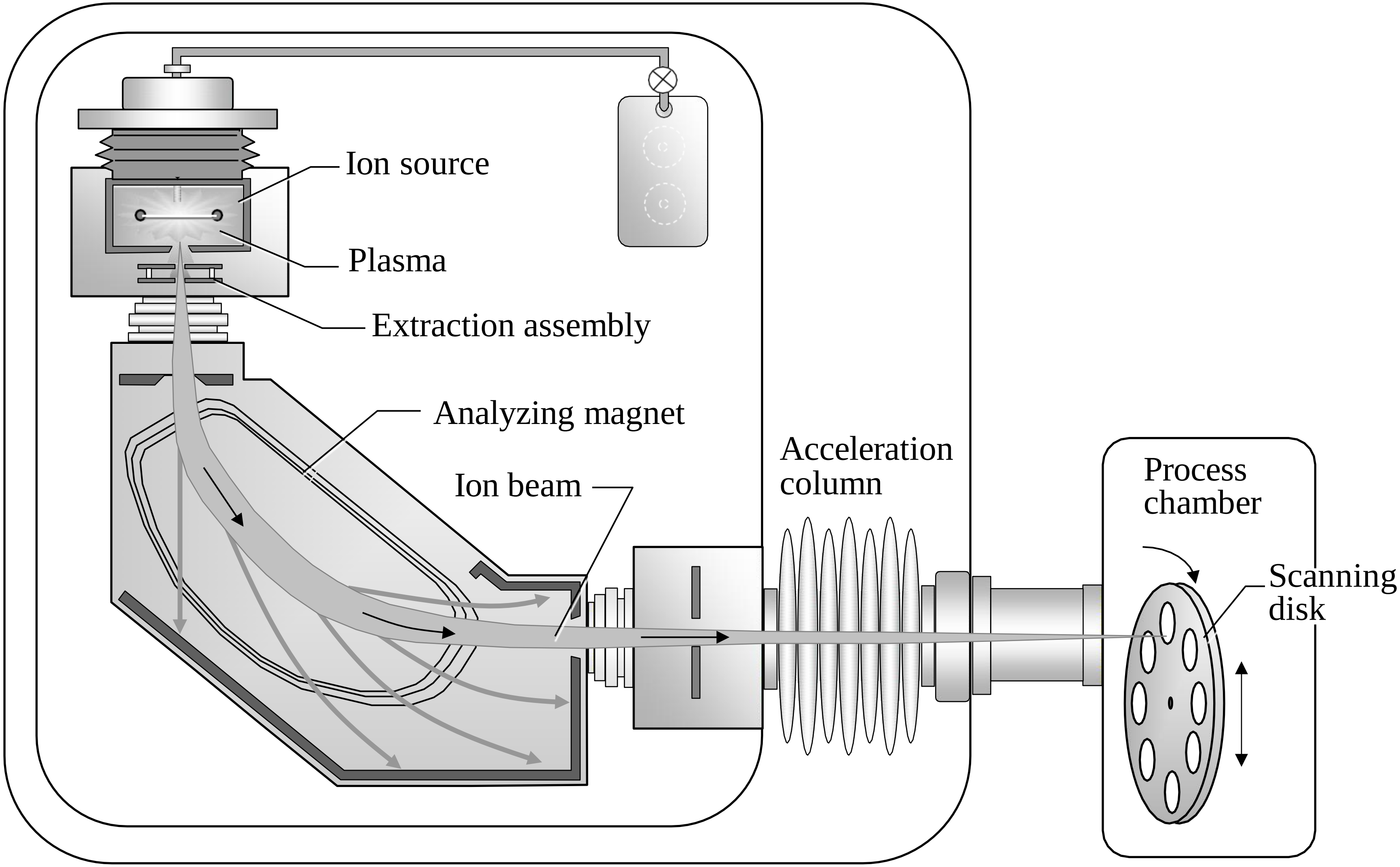
Controlling Dopant Concentration and Depth



a) Low dopant concentration (n^-, p^-) and shallow junction (x_j)

b) High dopant concentration (n^+, p^+) and deep junction (x_j)

General Schematic of an Ion Implanter



Advantages of Ion Implantation

1. Precise Control of Dopant Concentration
2. Good Dopant Uniformity
3. Good Control of Dopant Penetration Depth
4. Produces a Pure Beam of Ions
5. Low Temperature Processing
6. Ability to Implant Dopants Through Films
7. No Solid Solubility Limit

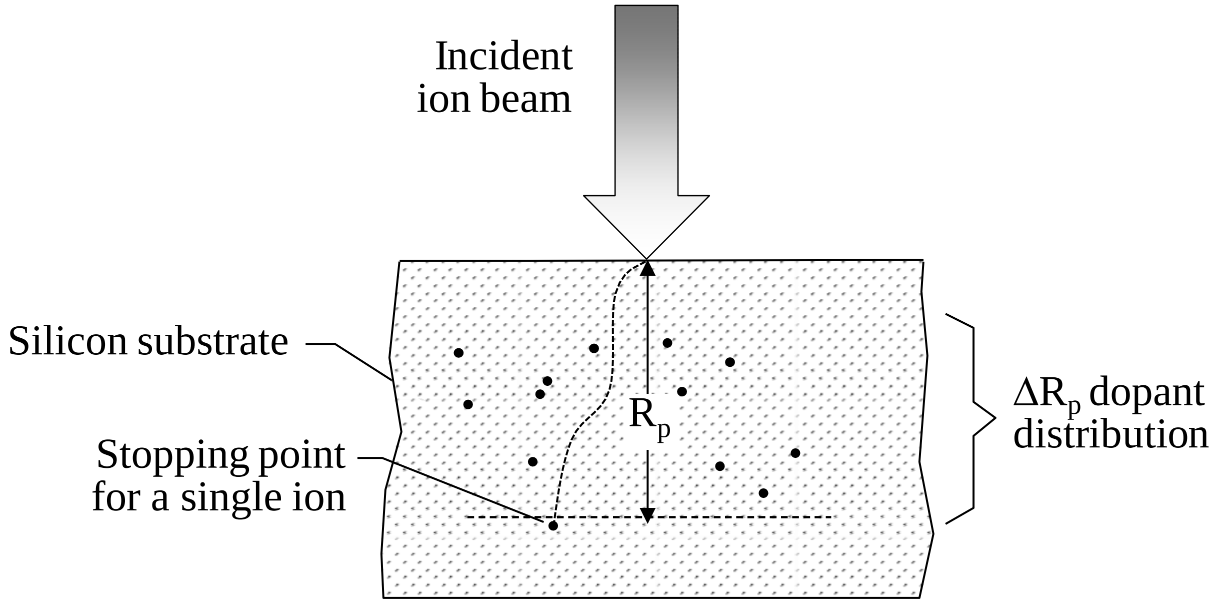
Table 17.5

Classes of Implanters

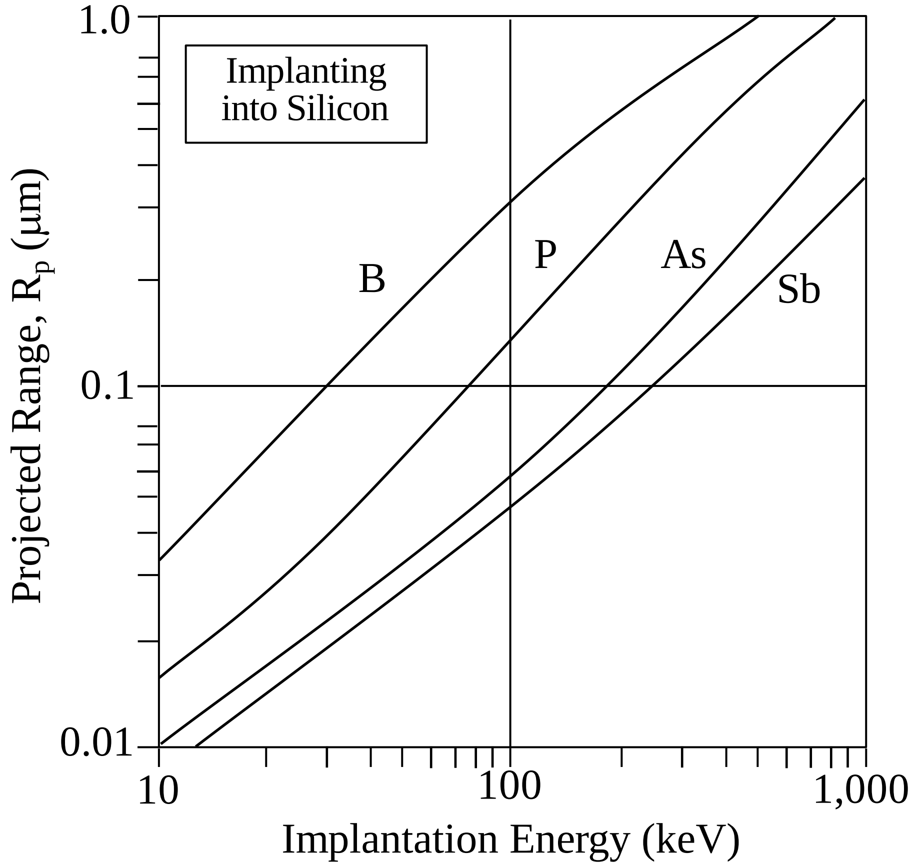
Class of Implante r System	Description and Applications
Medium Current	• Highly pure beam currents <10 mA. • Beam energy is usually < 180 keV. • Most often the ion beam is stationary and the wafer is scanned. • Specialized applications of punchthrough stops.
High Current	• Generate beam currents > 10 mA and up to 25 mA for high dos e implants. • Beam energy is usually <120 keV. • Most often the wafer is stationary and the ion beam does t he scanning. • Ultralow-energy beams (<4keV down to 200 eV) for implantin g ultrashallow source/drain junctions.
High Energy	• Beam energy exceeds 200 keV up to several MeV. • Place dopants beneath a trench or thick oxide layer. • Able to form retrograde wells and buried layers.
Oxygen Ion Implanters	• Class of high current systems used to implant oxygen in silico n- on-insulator (SOI) applications.

Table 17.6

Range and Projected Range of Dopant Ion

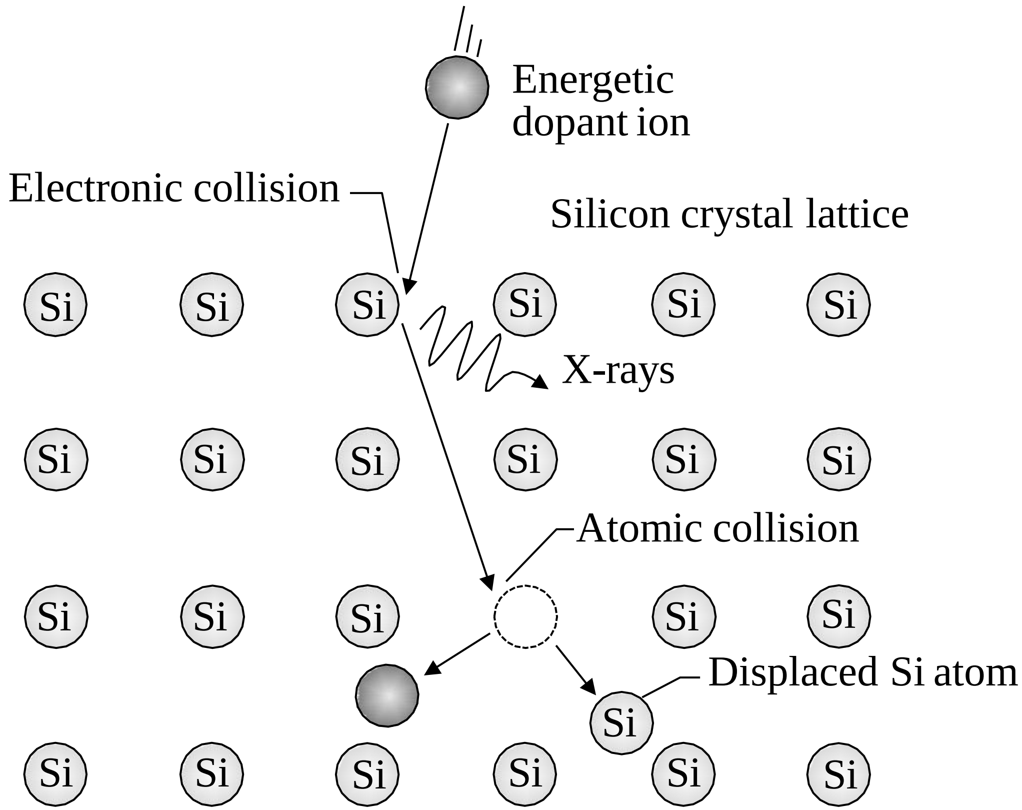


Projected Range Chart

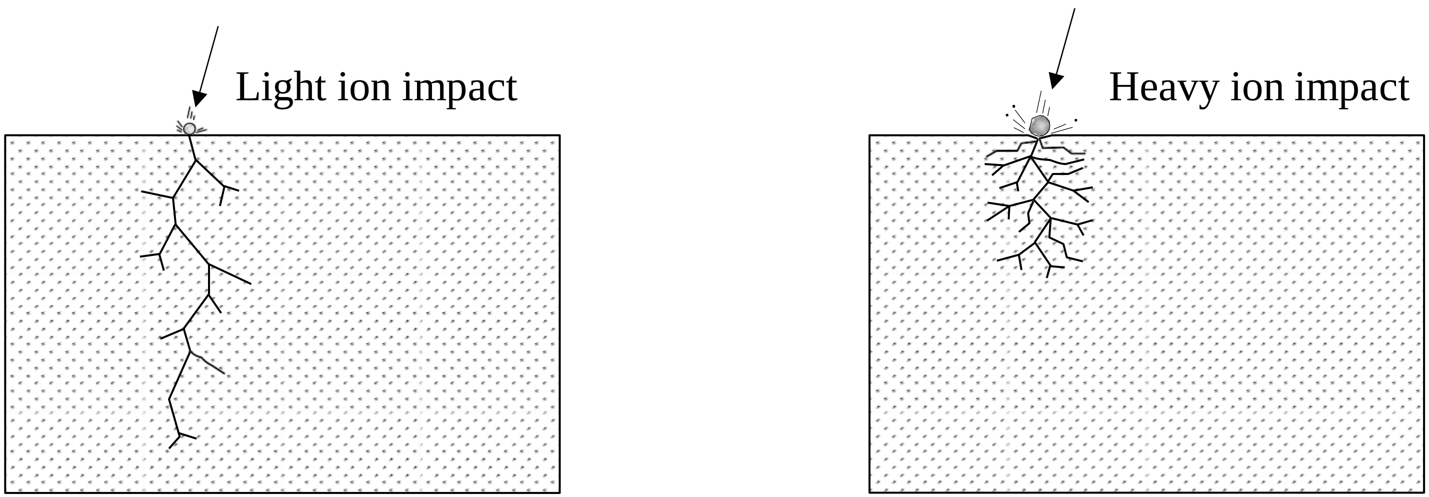


Redrawn from B.El-Kareh, *Fundamentals of Semiconductor Processing Technologies*, (Boston: Kluwer, 1995), p. 388

Energy Loss of an Implanted Dopant Atom



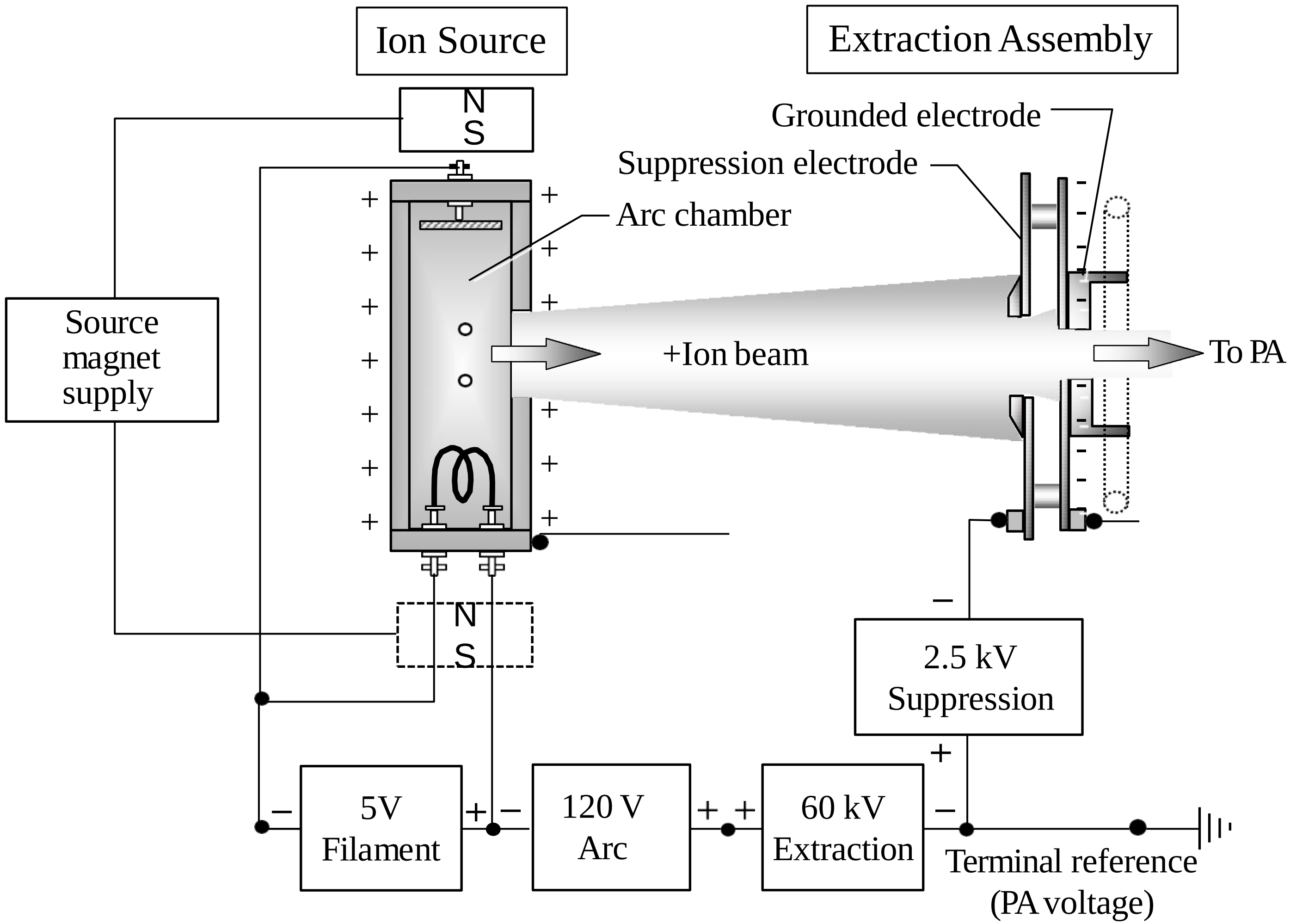
Crystal Damage Due to Light and Heavy Ions



Ion Implanters

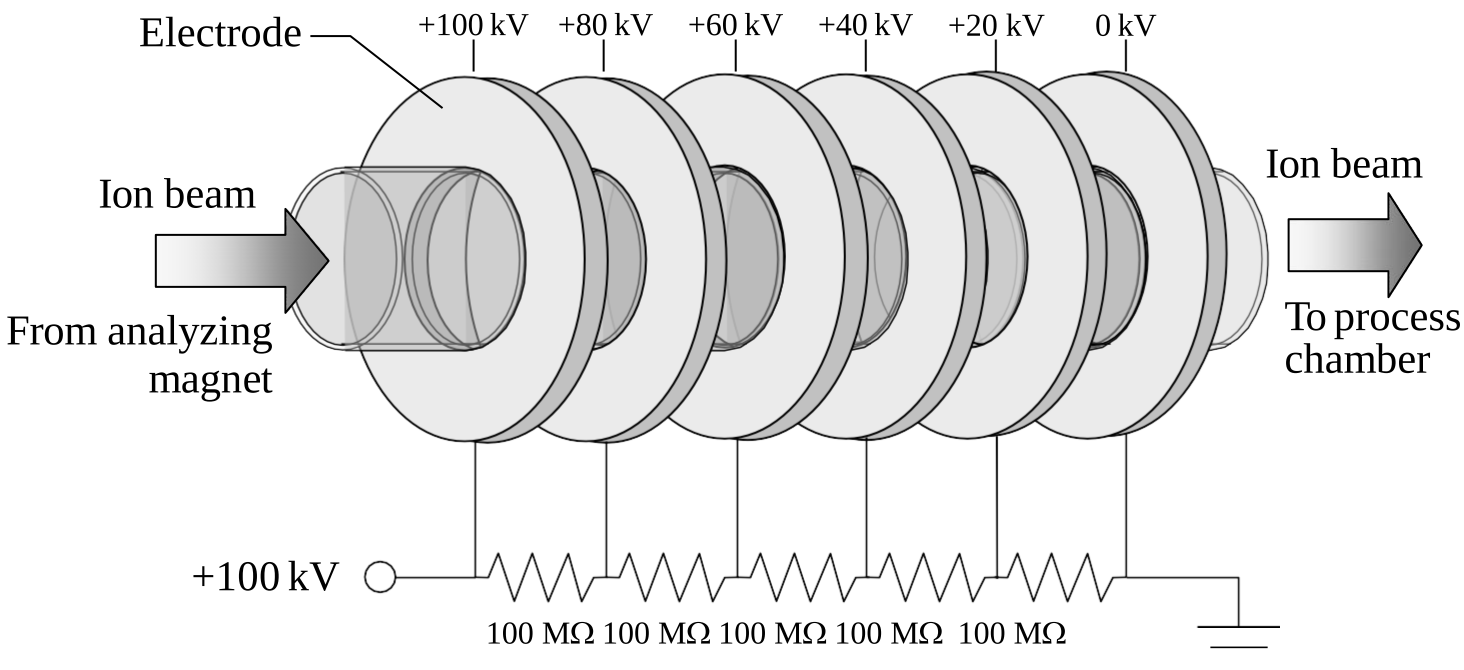
- Ion Source
- Extraction and Ion Analyzer
- Acceleration Column
- Scanning System
- Process Chamber
- Annealing
- Channeling
- Particles

Interaction of ion Source and Extraction Assemblies

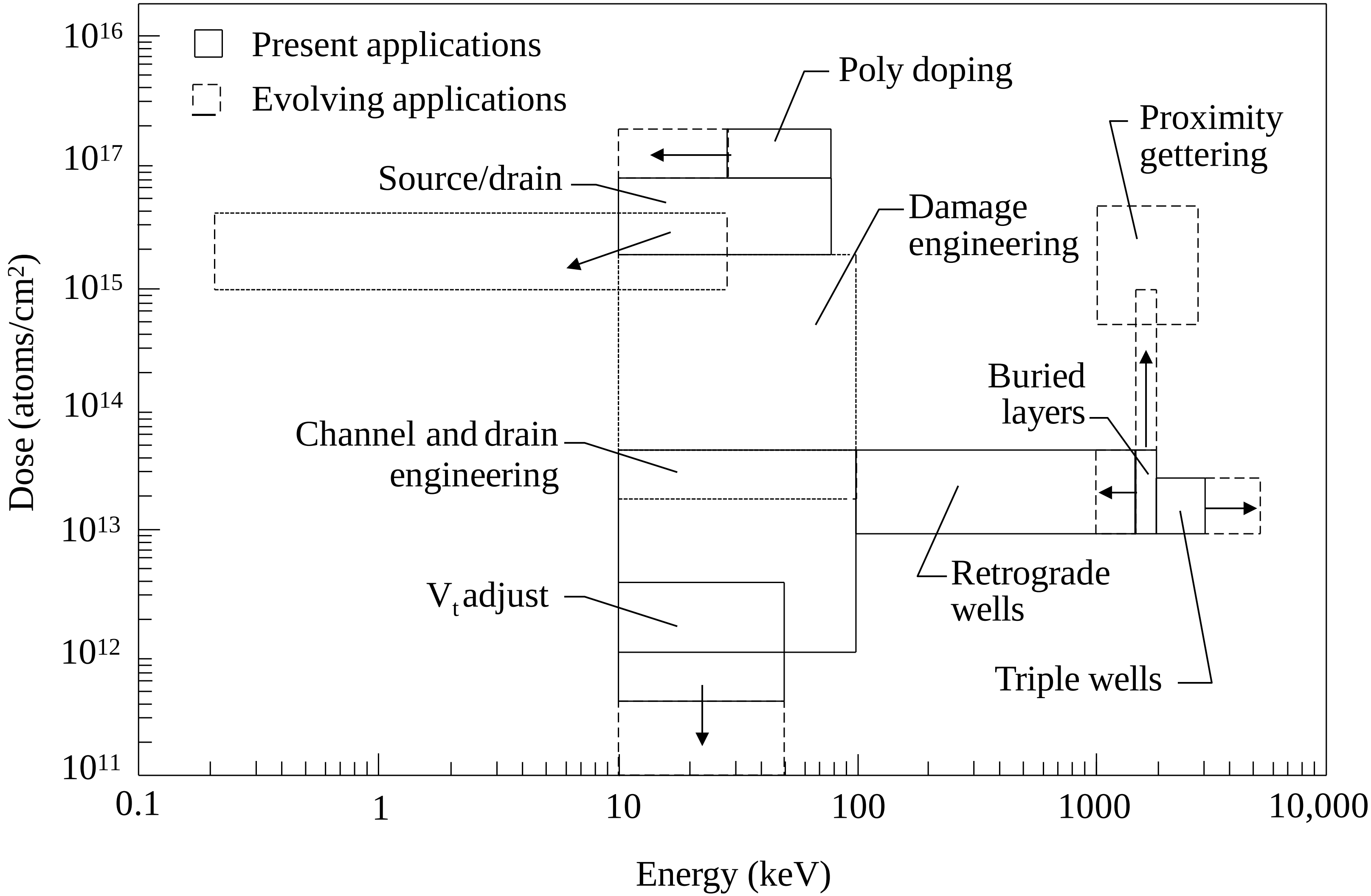


Used with permission from Applied Materials Technology, Precision Implanter 9500

Acceleration Column

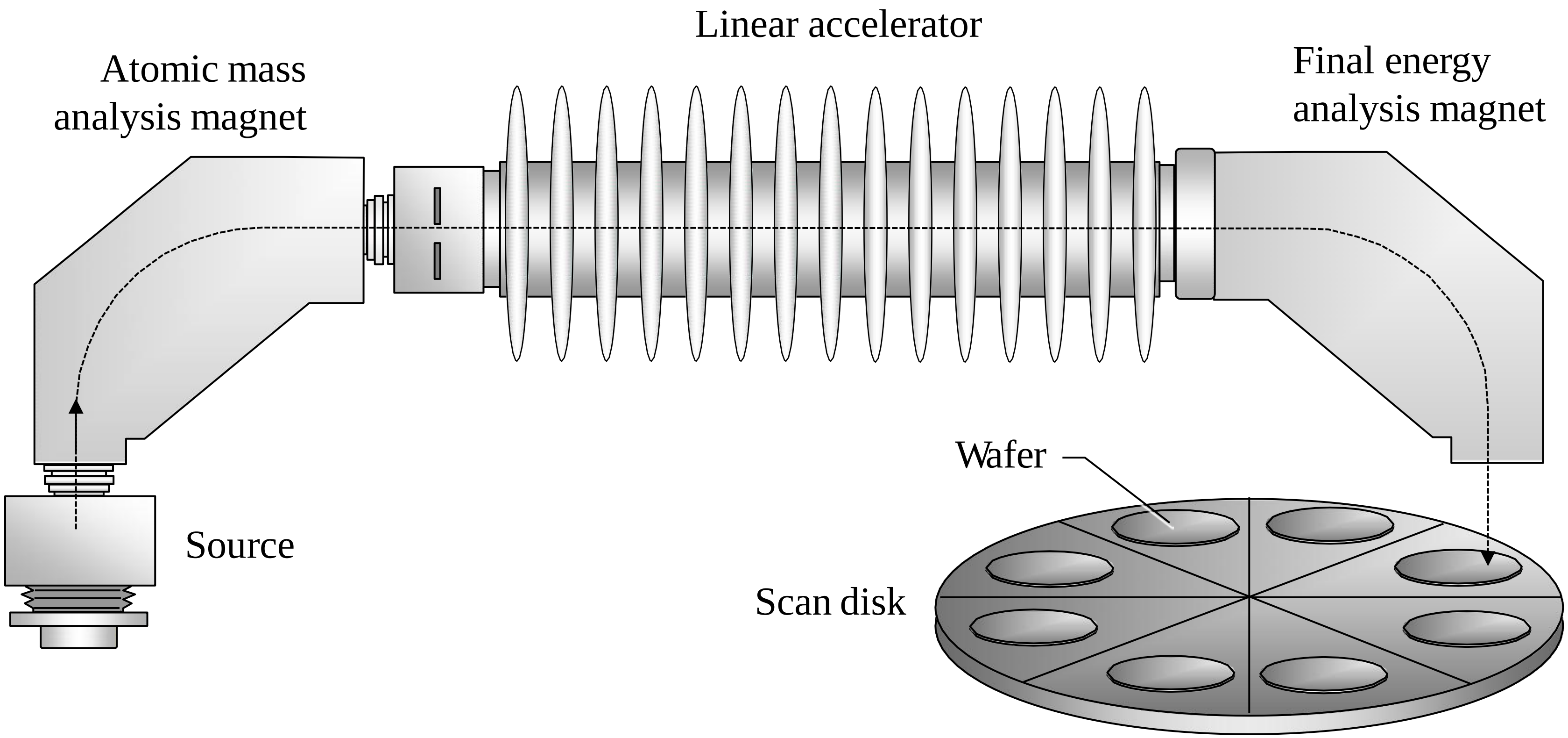


Dose Versus Energy Map

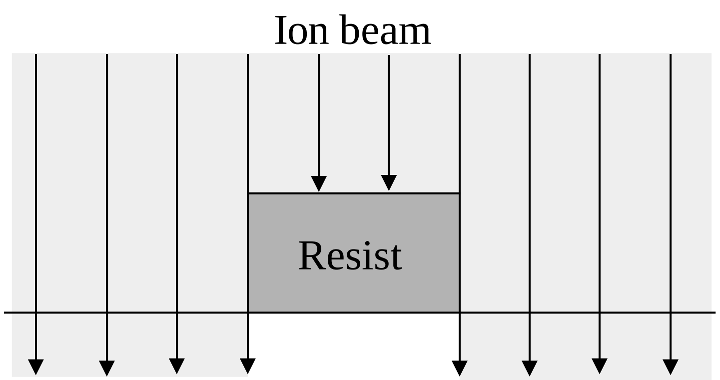


Used with permission from Varian Semiconductor Equipment

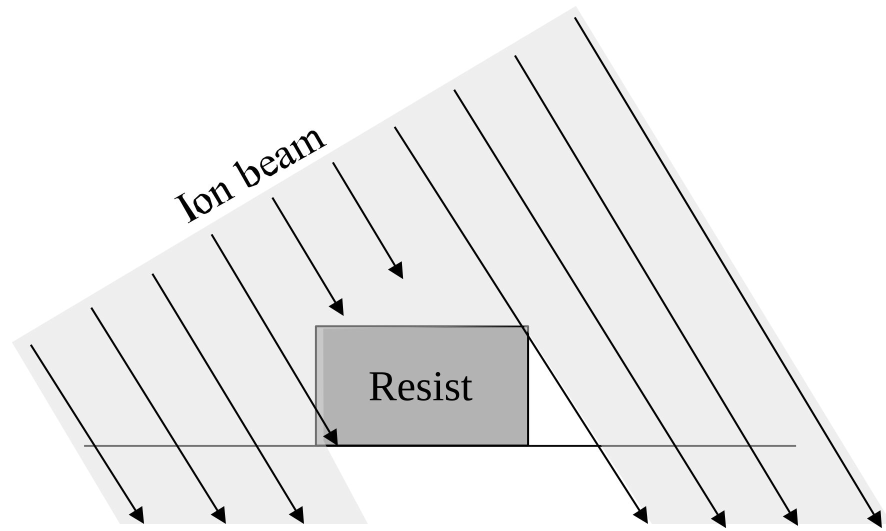
Linear Accelerator for High-Energy Implanters



Implant Shadowing

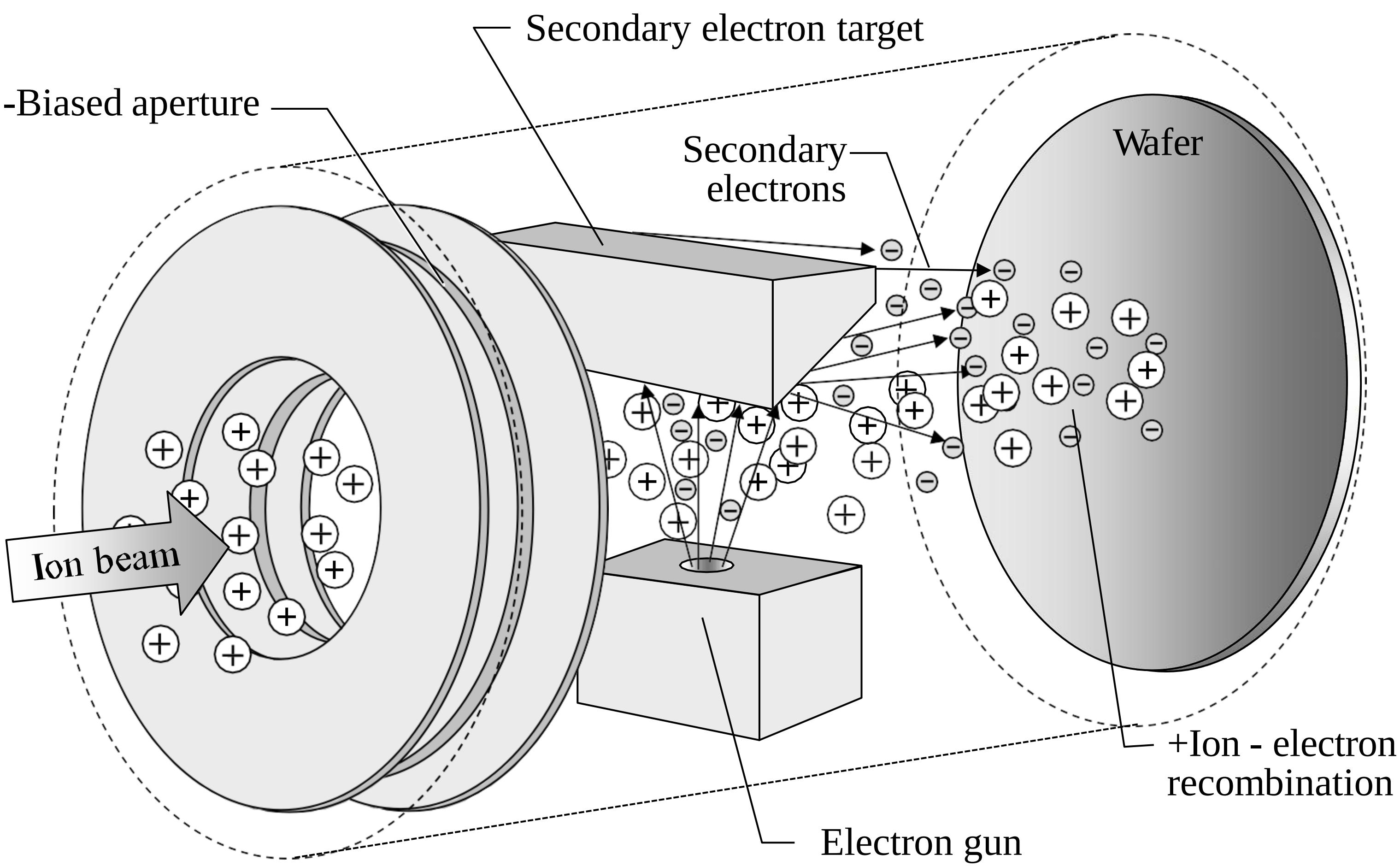


a) Mechanical scanning with no tilt



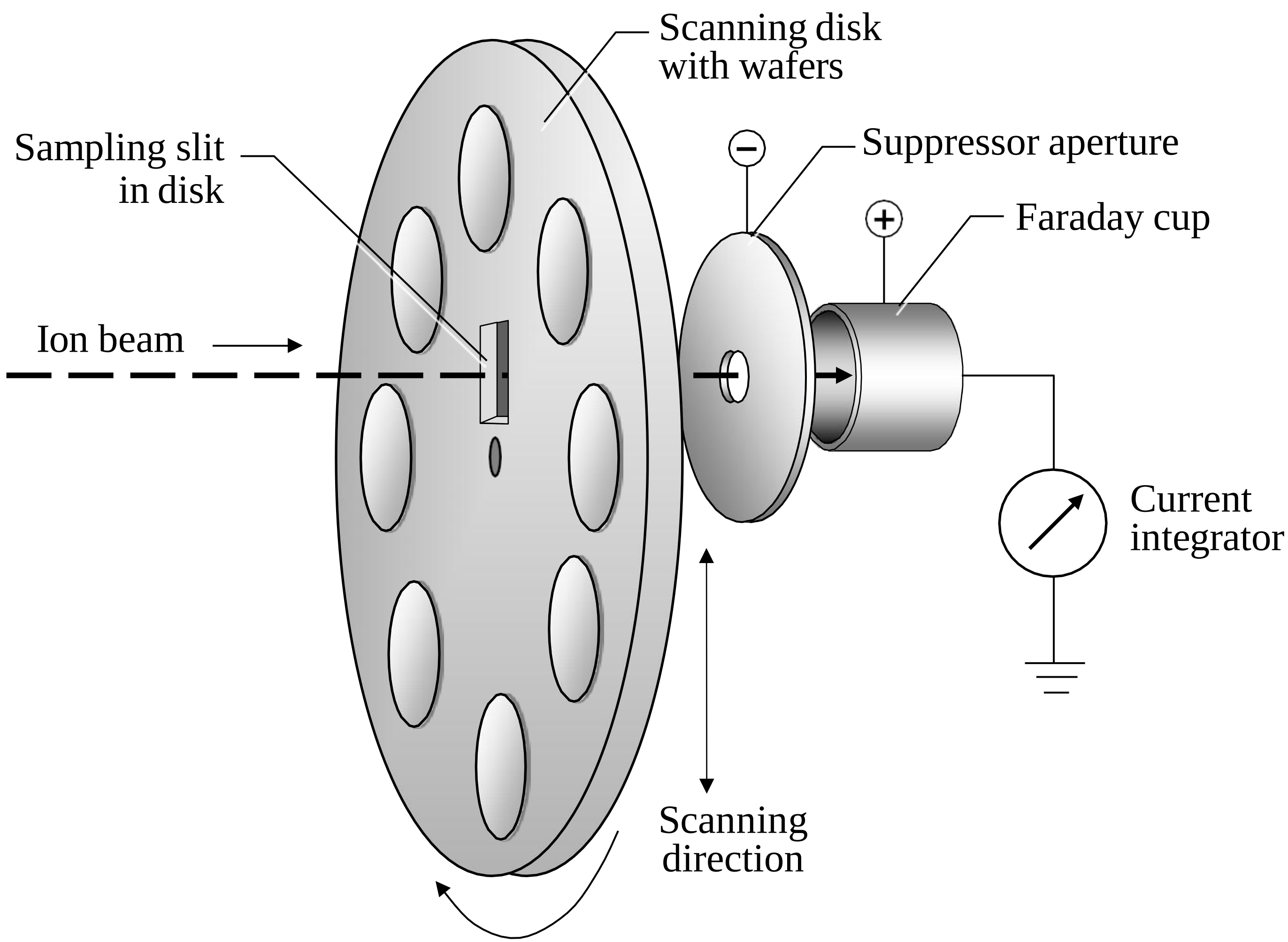
b) Electrostatic scanning with normal tilt

Electron Shower for Wafer Charging Control



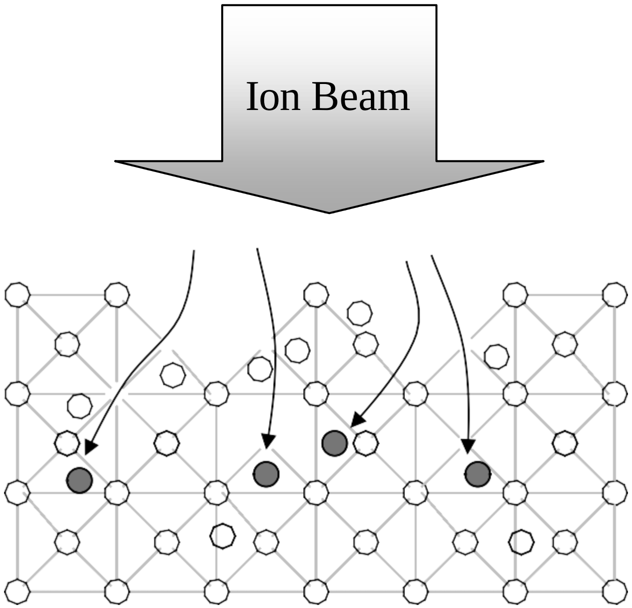
Adapted from Eaton NV10 ion implanter, circa 1983

Faraday Cup Beam Current Measurement



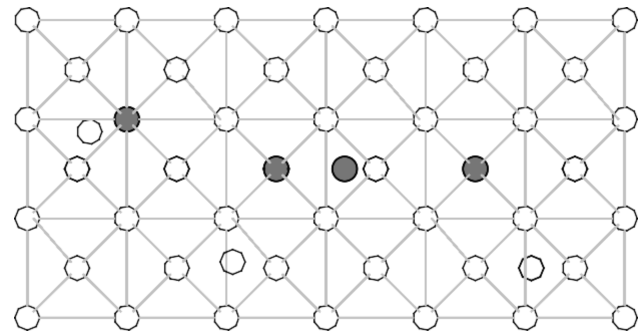
Redraawn from S. Ghandhi, VLSI Fabricaton Principles: Silicon and Gallium Arsenide, 2d ed., (New York: Wiley, 1994), p. 417

Annealing of Silicon Crystal



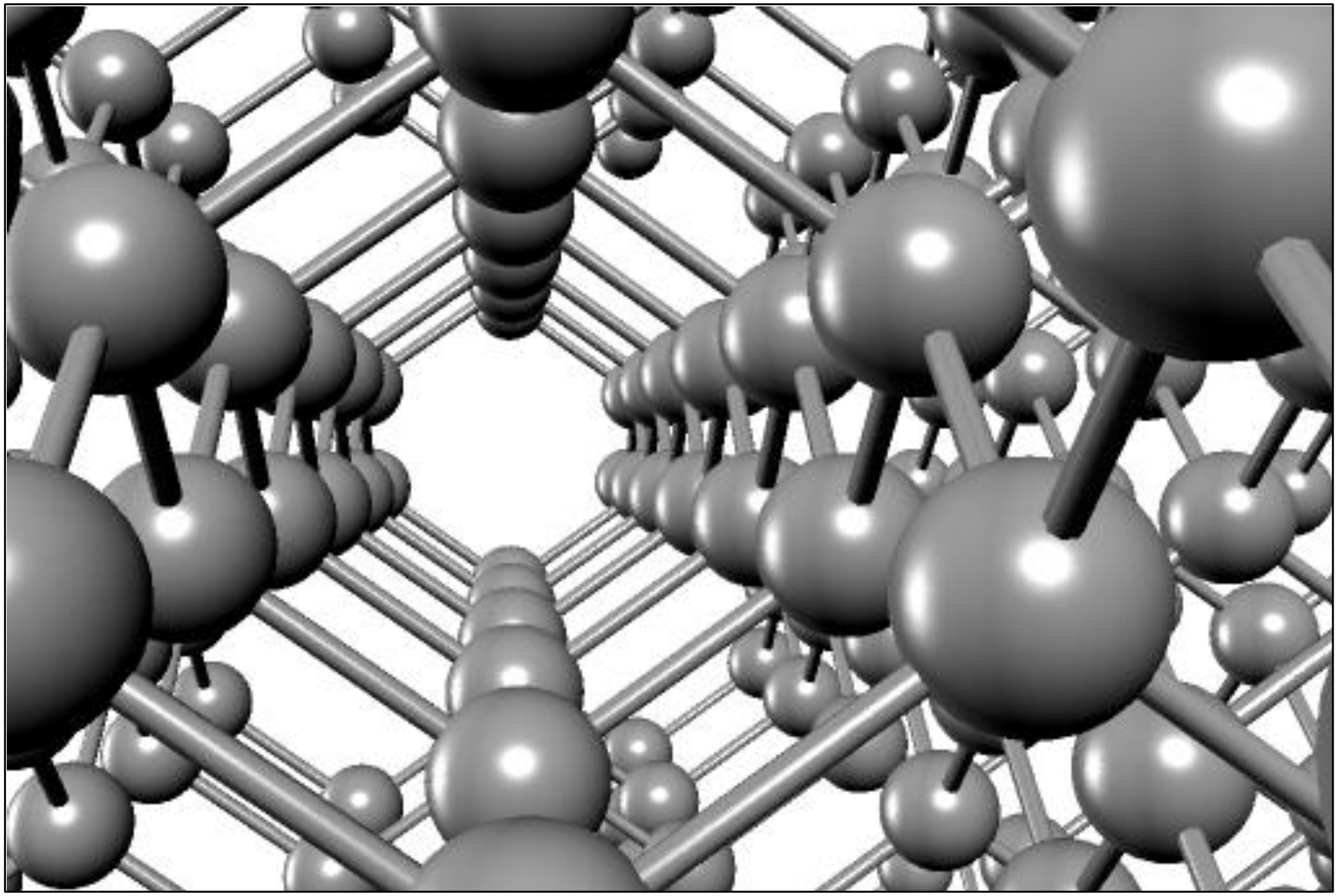
a) Damaged Si lattice during implant

Repaired Si lattice structure and activated dopant-silicon bonds



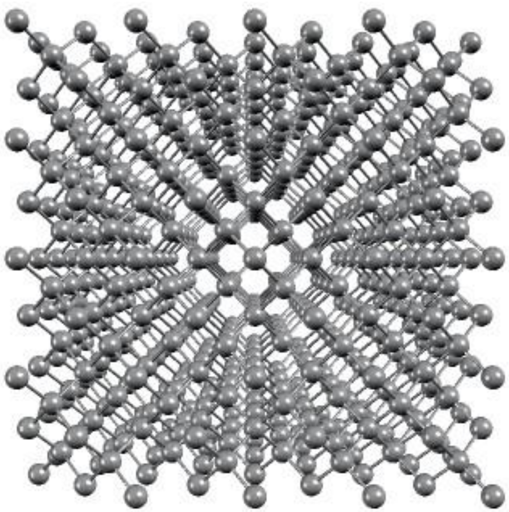
b) Si lattice after annealing

Silicon Lattice Viewed Along <110> Axis

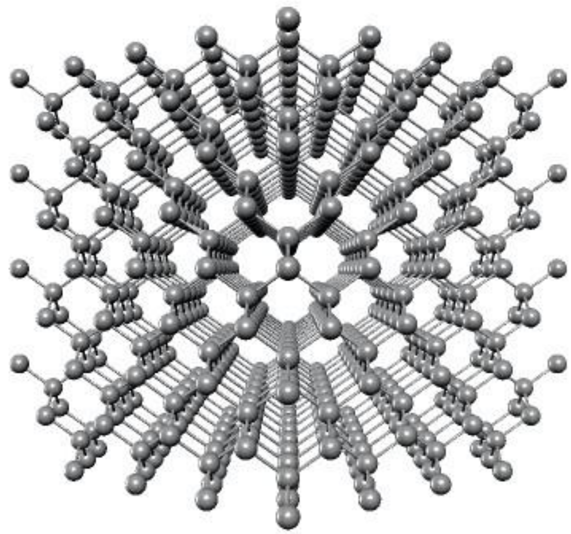


Used with permission from Edgard Torres Designs

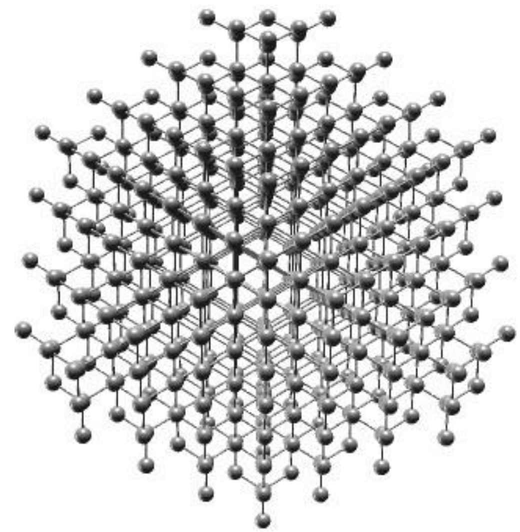
Ion Entrance Angle and Channeling



<100>



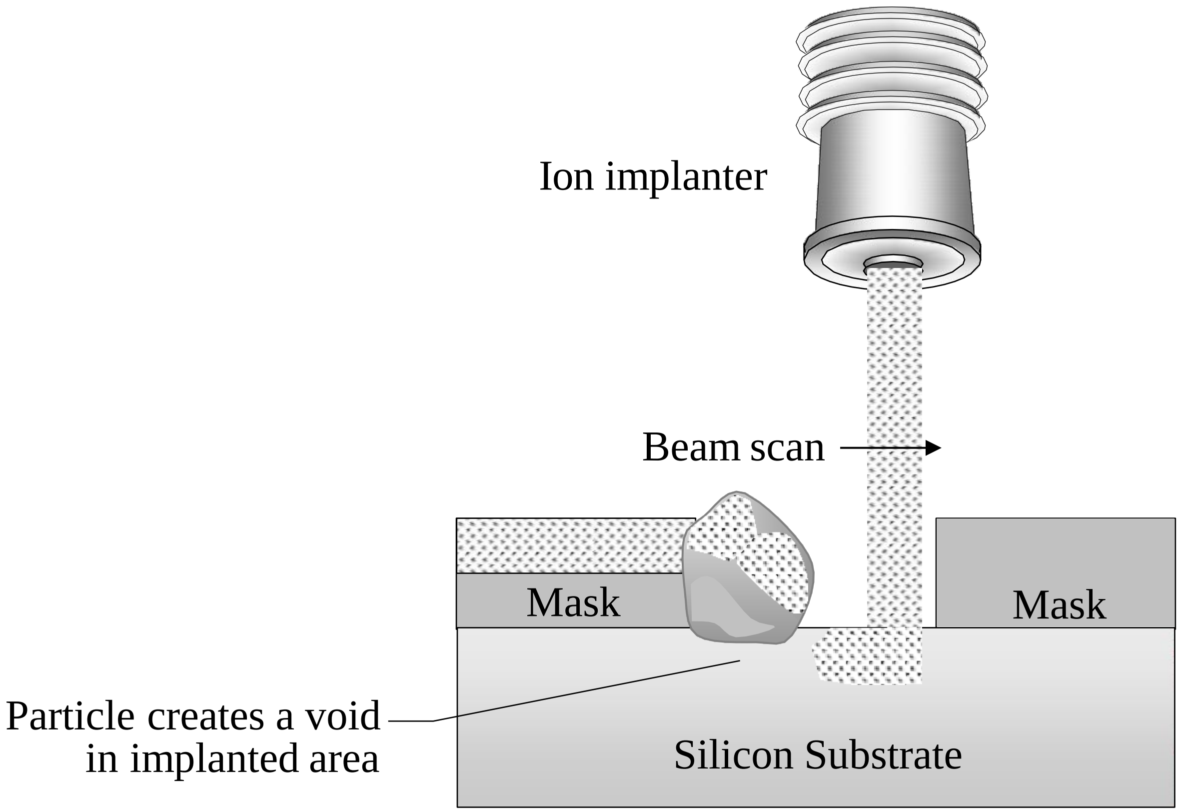
<110>



<111>

Used with permission from Edgard Torres Designs

Implantation Damage from Particulate Contamination

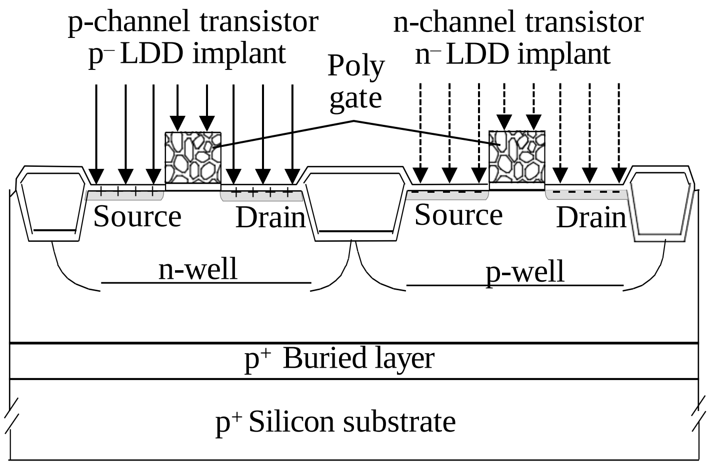


Ion Implant Trends in Process Integration

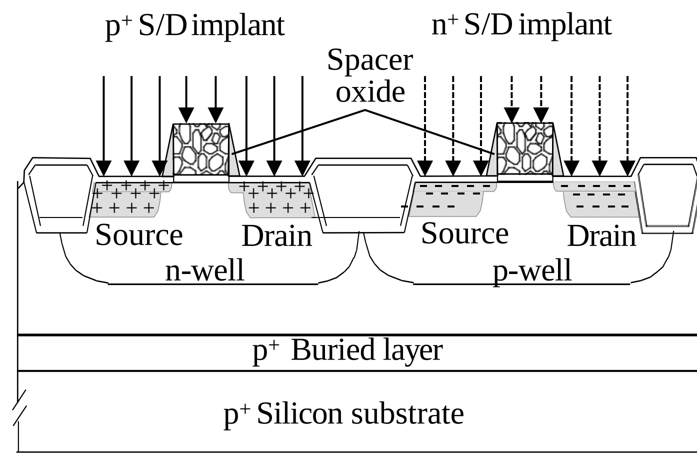
Examples of Different Implant Processes

- Deep buried layers
- Retrograde wells
- Punchthrough stoppers
- Threshold voltage adjustment
- Lightly doped drain (LDD)
- Source/drain implants
- Polysilicon gate
- Trench capacitor
- Ultra-shallow junctions
- Silicon on Insulator (SOI)

Source-Drain Formations

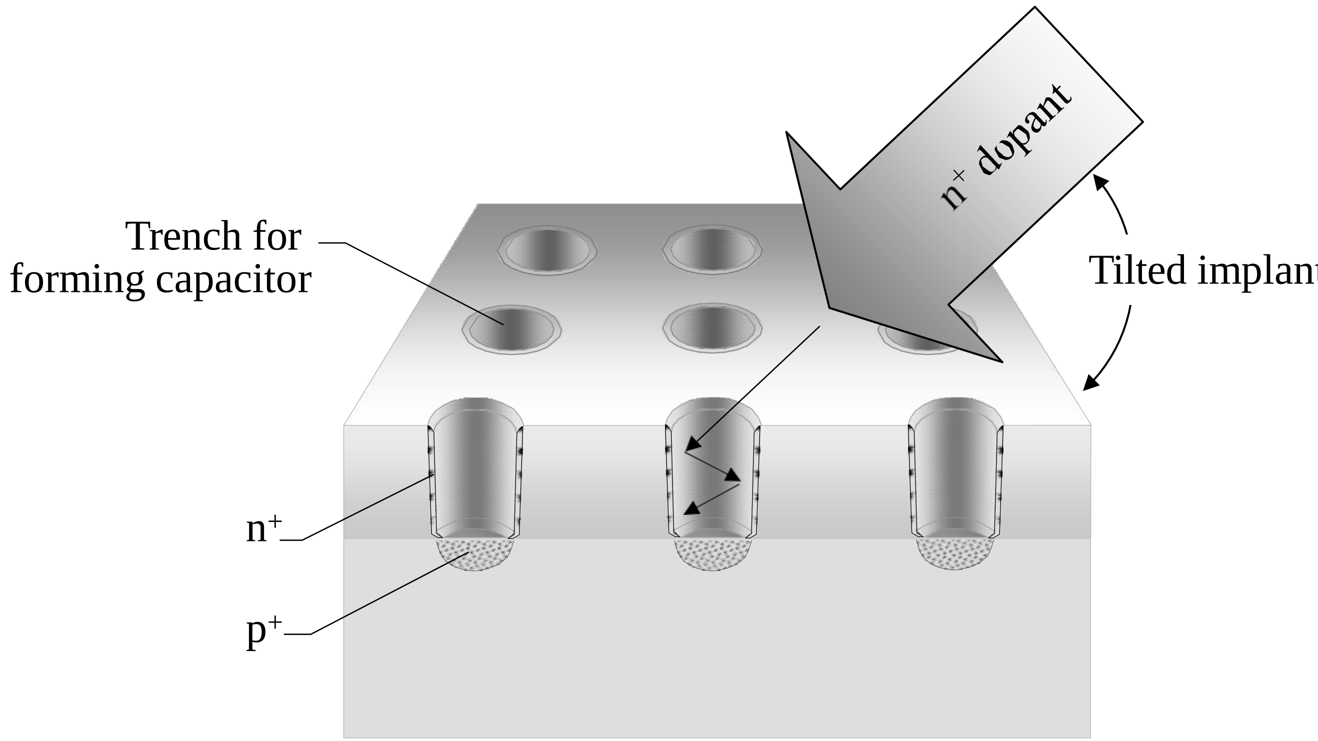


a) p^- and n^- lightly-doped drain implants
(performed in two separate operations)



b) p^+ and n^+ Source/drain implants
(performed in two separate operations)

Dopant Implant on Vertical Sidewalls of Trench Capacitor



End of Slide