Next generation semiconductor devices and applications

(차세대 반도체 소자 및 응용)

장소: 공과대학 6호관 510호
시간: 화 (6-A, 6-B, 7-A, 7-B, 8-A, 8-B)

5. Next generation electronic devices

Organic Non-volatile Memory

Organic Resistive Switching Memory
(Simple & Advanced Architecture)

Memory and Logic Will Play a Critical Role in Future Printed Electronics Applications

Smart tagging of "everything"

Memory and logic enable integrated systems

(e.g., store max/min temperature, turn power on/off etc.)

Large area displays, disposable price displays and lighting

Disposable sensors/tags

From THINFILM

Organic Non-volatile Memory Devices (resistive change type)

Organic memory refers to devices that are used to store data or programs on a temporary or permanent basis using organic materials as an active layer.

Usage of organic memory devices

> "Deposited on top of flexible plastic materials, plastic circuitry could, for instance, be built into flexible displays and packed into smaller spaces inside cellphones, MP3players, plastic RFID tags and even credit cards."

> "The time for OMDs might finally be at hand ... even if the first application is the humble **radio-frequency identification (RFID) tags** used in retail store product."

From "TechNewsWorld 2011"

Merits

- Simple structure
- Easy of fabrication
- Compatibility with flexible substrates
- Comparative low cost
- Multilayer stacking

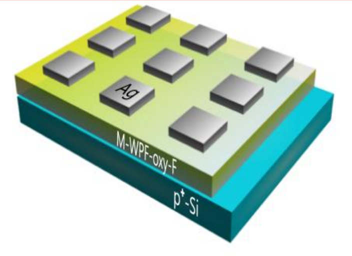
Challenges

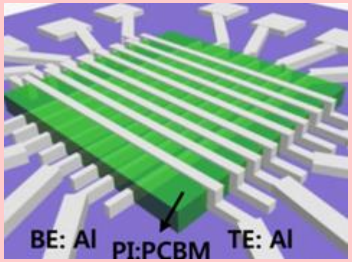
- Unknown switching mechanism
- Unstable in ambient condition
- Data retention time
- Reliability
- **Processability** → **UV patterning & cross-linking**
- **Integration** → **Cross-bar structure**
- **Novel architecture** → **1D-1R or 1T-1R architecture**

Family Tree of Organic Non-volatile Memory

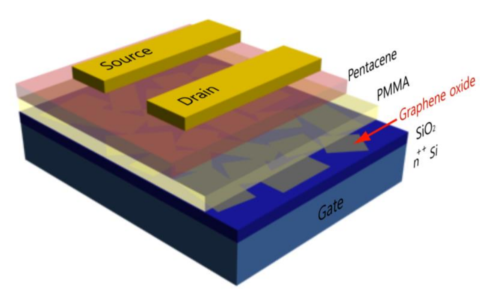
Organic Non-volatile Memory

- Organic memory devices
  - Non-Volatile
    - Resistive change
      - MIM type
      - Cross-bar type
        - 1T-1R
        - 1D-1R
        - 3D stacking
    - Charge trap, Ferroelectric
      - TFT type
  - Volatile





Two terminal device
-Top electrode
-Bottom electrode

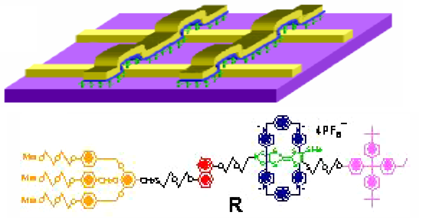


Three terminal device
-Gate
-Source
-Drain

Types of Organic Non-volatile Memory

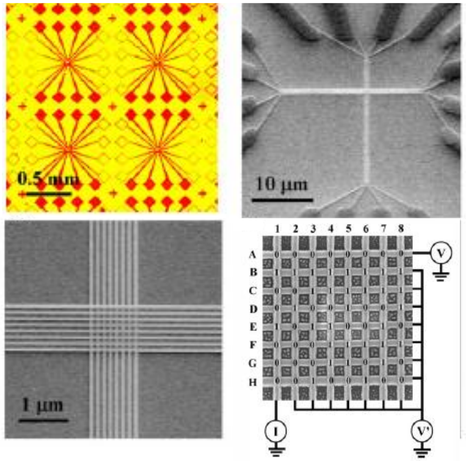
Resistive change type

Molecular Memory



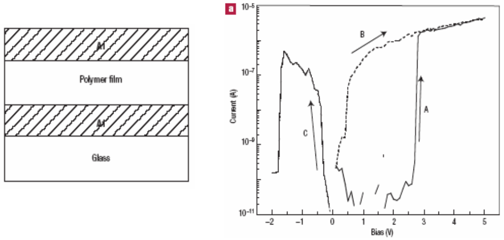
- Rotaxane molecular film
- Layer thickness ~ 2 nm

6.4 Gbit/cm²

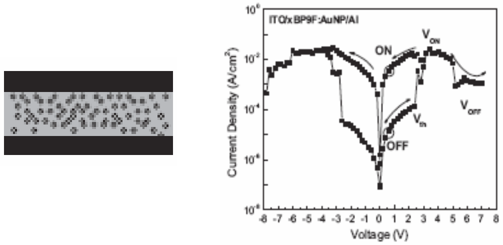


Chen *et al*, *Nanotechnology* 14, 462 (**2003**)

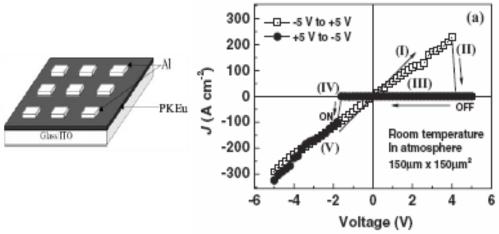
Polymer Memory



Ouyang *et al*, *Nat. Mater.* 3, 918 (**2004**)



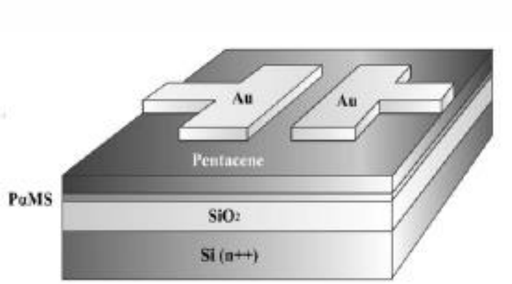
Bozano *et al*, *Adv. Func. Mater.* 15, 1933 (**2005**)

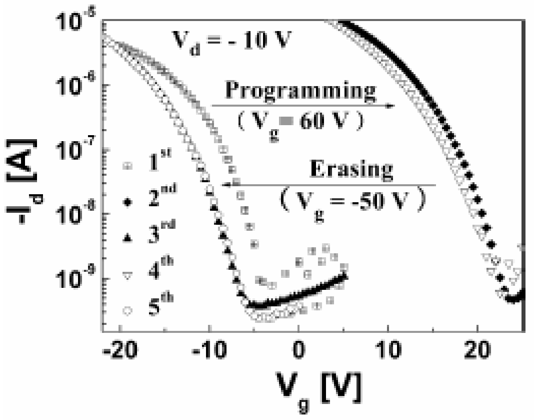


Ling *et al*, *Adv. Mater.*, 17, 455 (**2005**)

Flash type

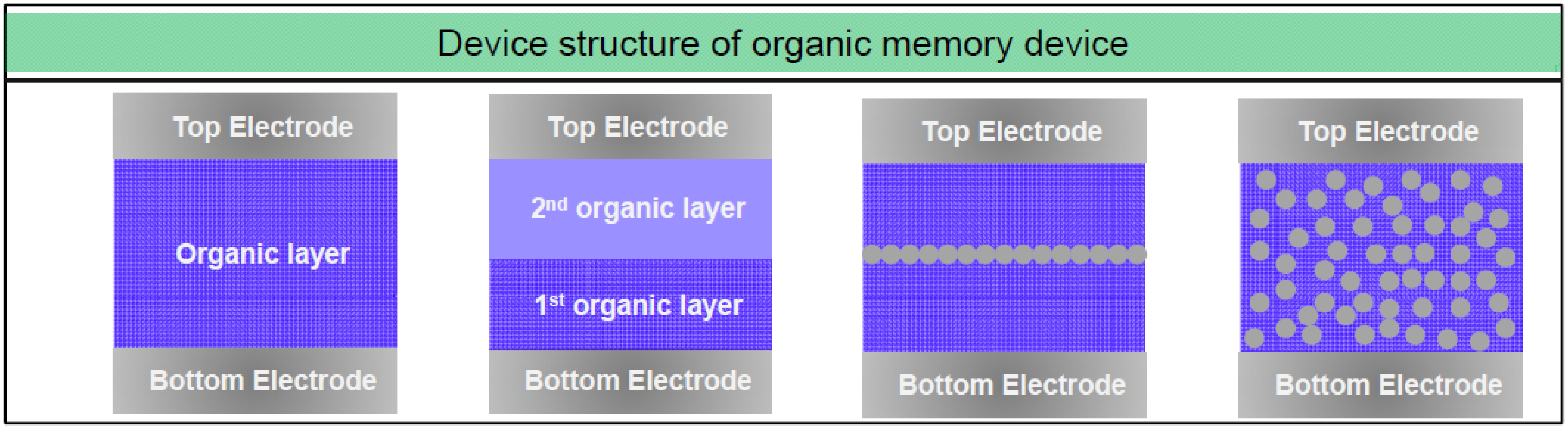
charge trap memory

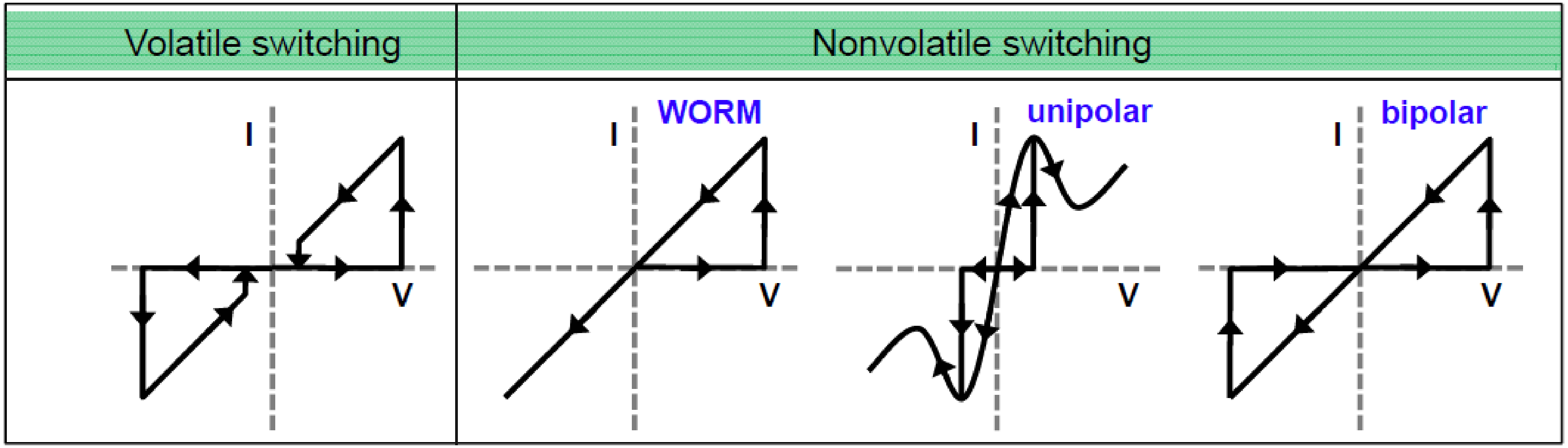




Beag *et al*, *Adv. Mater.* 18, 3179 (**2006**)

Organic memory devices


Device structure of organic memory device


Volatile switching

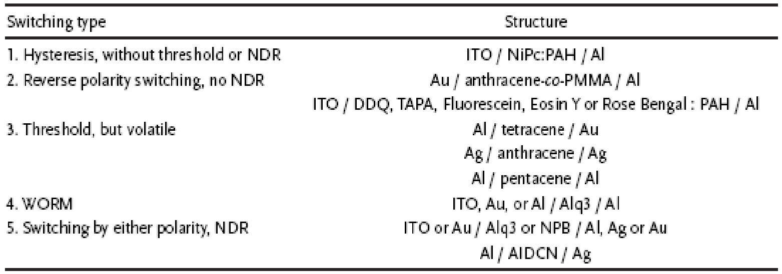
Nonvolatile switching

Scott *et al*, ***Adv. Mater.*** 19, 1452 (2007)

Materials for Organic Non-volatile Memory

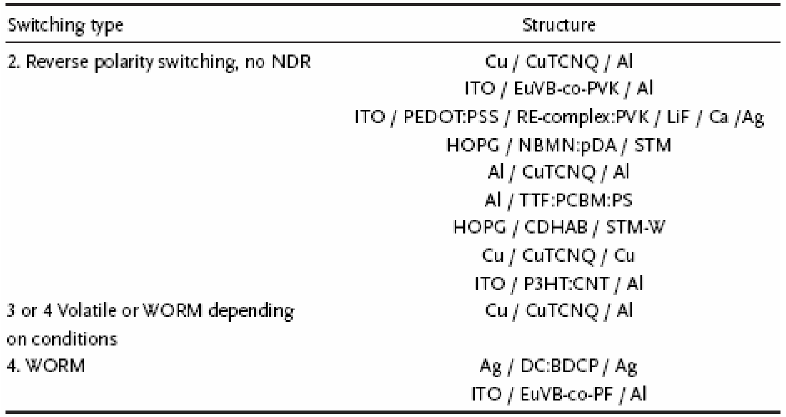
- Organic materials for resistive change memory devices

Small molecule



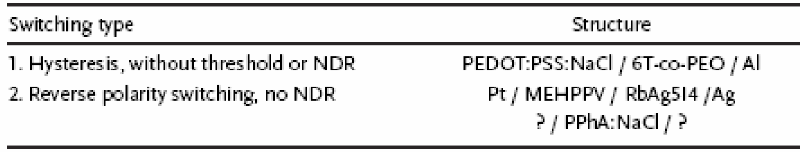
Switching type	Structure
1. Hysteresis, without threshold or NDR	ITO / NiPc:PAH / Al
2. Reverse polarity switching, no NDR	Au / anthracene-*co*-PMMA / Al
	ITO / DDQ, TAPA, Fluorescein, Eosin Y or Rose Bengal : PAH / Al
3. Threshold, but volatile	Al / tetracene / Au
	Ag / anthracene / Ag
	Al / pentacene / Al
4. WORM	ITO, Au, or Al / Alq3 / Al
5. Switching by either polarity, NDR	ITO or Au / Alq3 or NPB / Al, Ag or Au
	Al / AIDCN / Ag

Donor-acceptor complexes



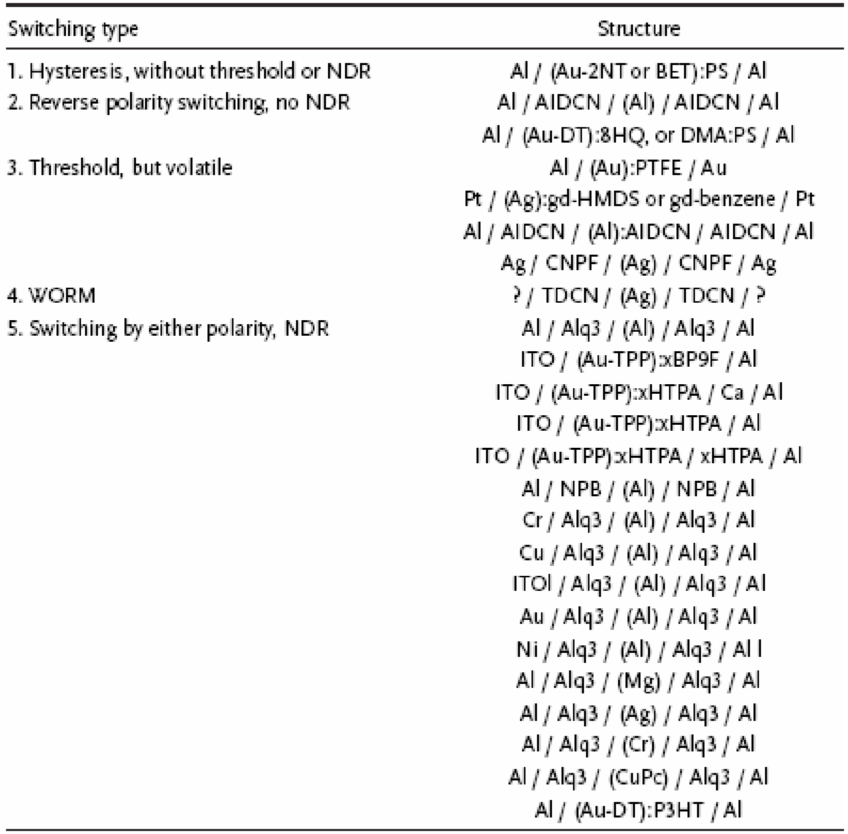
Switching type	Structure
2. Reverse polarity switching, no NDR	Cu / CuTCNQ / Al
	ITO / EuVB-co-PVK / Al
	ITO / PEDOT:PSS / RE-complex:PVK / LiF / Ca /Ag
	HOPG / NBMN:pDA / STM
	Al / CuTCNQ / Al
	Al / TTF:PCBM:PS
	HOPG / CDHAB / STM-W
	Cu / CuTCNQ / Cu
	ITO / P3HT:CNT / Al
3 or 4 Volatile or WORM depending on conditions	Cu / CuTCNQ / Al
4. WORM	Ag / DC:BDCP / Ag
	ITO / EuVB-co-PF / Al

Mobile-ion, electrochemical system



Switching type	Structure
1. Hysteresis, without threshold or NDR	PEDOT:PSS:NaCl / 6T-co-PEO / Al
2. Reverse polarity switching, no NDR	Pt / MEHPPV / RbAg5I4 /Ag
	? / PPhA:NaCl / ?

Nanoparticle blends

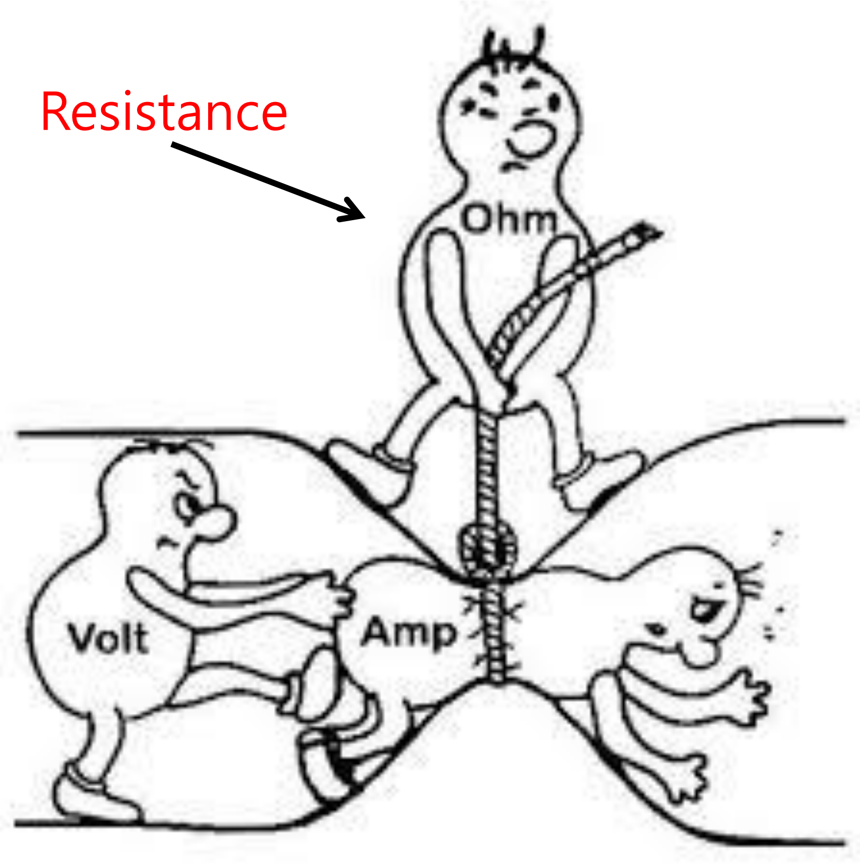


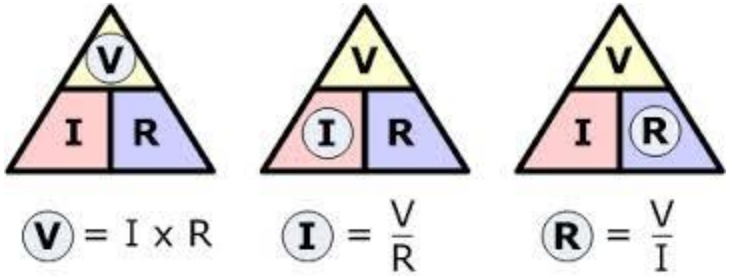
Switching type	Structure
1. Hysteresis, without threshold or NDR	Al / (Au-2NT or BET):PS / Al
2. Reverse polarity switching, no NDR	Al / AIDCN / (Al) / AIDCN / Al
	Al / (Au-DT):8HQ, or DMA:PS / Al
3. Threshold, but volatile	Al / (Au):PTFE / Au
	Pt / (Ag):gd-HMDS or gd-benzene / Pt
	Al / AIDCN / (Al):AIDCN / AIDCN / Al
	Ag / CNPF / (Ag) / CNPF / Ag
4. WORM	? / TDCN / (Ag) / TDCN / ?
5. Switching by either polarity, NDR	Al / Alq3 / (Al) / Alq3 / Al
	ITO / (Au-TPP):xBP9F / Al
	ITO / (Au-TPP):xHTPA / Ca / Al
	ITO / (Au-TPP):xHTPA / Al
	ITO / (Au-TPP):xHTPA / xHTPA / Al
	Al / NPB / (Al) / NPB / Al
	Cr / Alq3 / (Al) / Alq3 / Al
	Cu / Alq3 / (Al) / Alq3 / Al
	ITOl / Alq3 / (Al) / Alq3 / Al
	Au / Alq3 / (Al) / Alq3 / Al
	Ni / Alq3 / (Al) / Alq3 / Al l
	Al / Alq3 / (Mg) / Alq3 / Al
	Al / Alq3 / (Ag) / Alq3 / Al
	Al / Alq3 / (Cr) / Alq3 / Al
	Al / Alq3 / (CuPc) / Alq3 / Al
	Al / (Au-DT):P3HT / Al

Scott *et al*, *Adv. Mater. 19*, 1452 (2007)

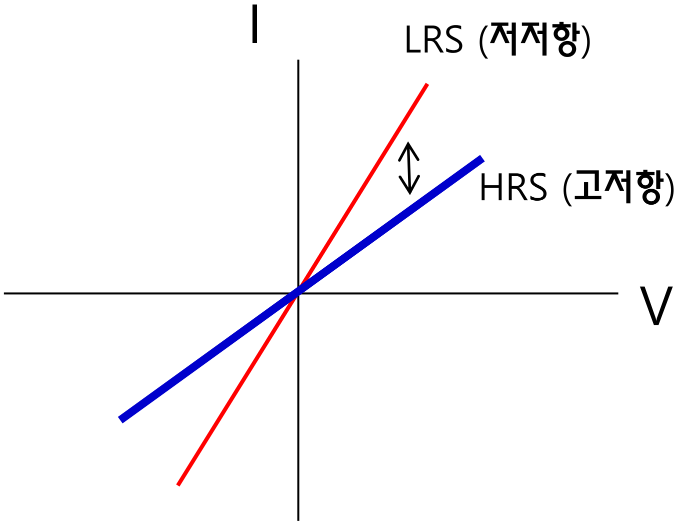
Working Principle of Organic Non-volatile Memory

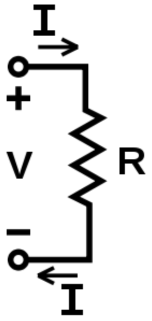
Ohm's Law





$V = I \times R$　　$I = \frac{V}{R}$　　$R = \frac{V}{I}$

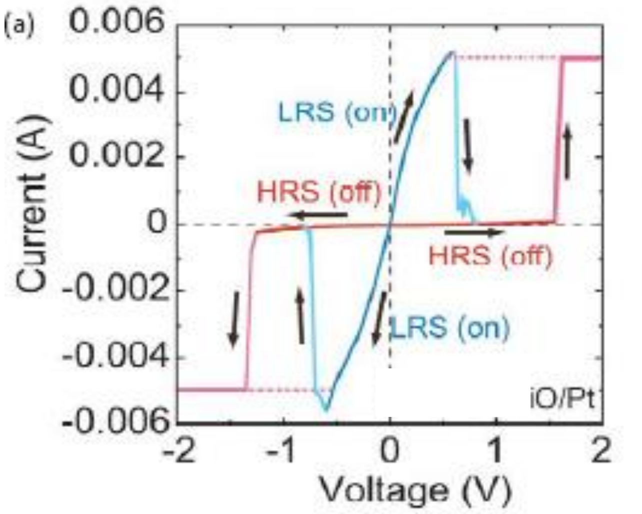




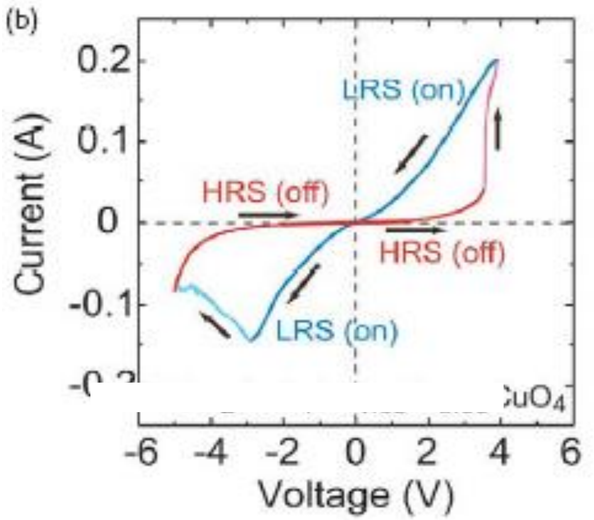
Working Principle of Organic Non-volatile Memory

- Switching type of organic memory device

- Unipolar switching



- Bipolar switching

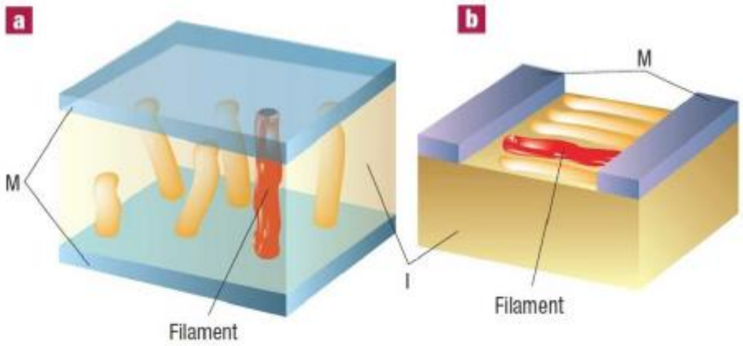


- Switching parameters

- Kind of materials
- Thickness of organic active layer
- Kind of metal electrodes
- Device architecture
- How to Measure-compliance current, sweep voltage, sweep direction

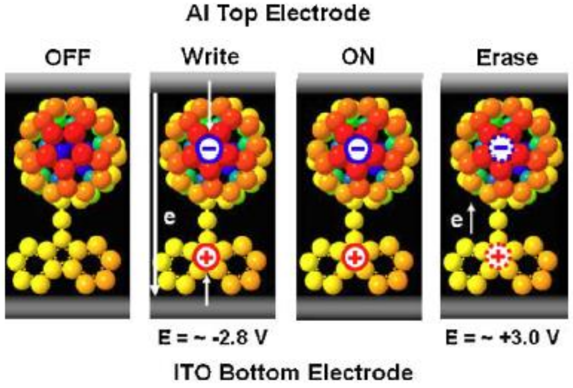
Mechanisms of Organic Non-volatile Memory

✓ Filamentary conduction



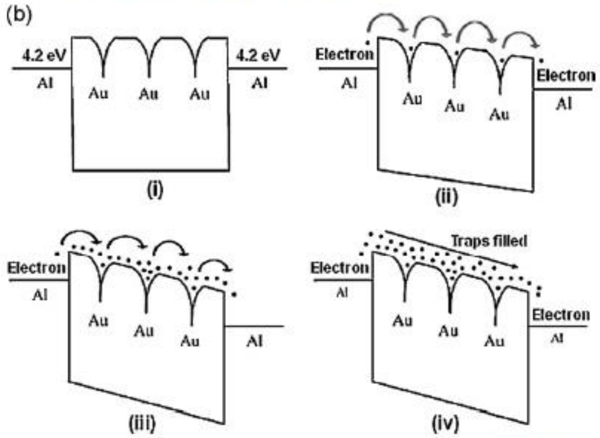
Nat. Mater. 6, 833 (2007)

✓ Charge-transfer



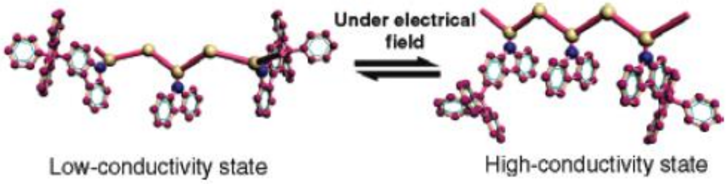
Langmuir, 23, 312 (2007)

✓ Space charge and traps



IEDL, 28, 569 (2007)

✓ Conformational Change



J. AM. CHEM. SOC. 130, 2120 (2008)

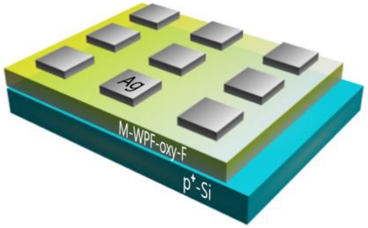
✓ Ionic conduction, tunneling effect, and etc

Research Summary of Organic Non-volatile Memory

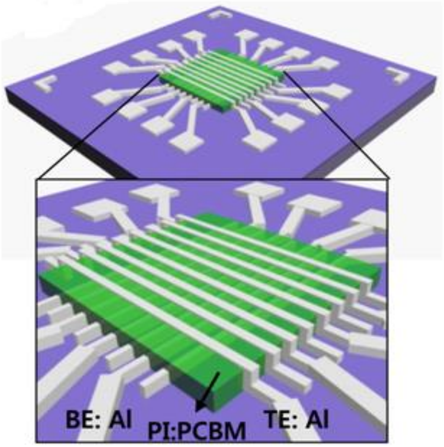
- Simple Architecture
  >>> MIM, Cross-bar

- Advanced Architectures for organic memory device
  >>> 1T-1R, 1D-1R, 3D stacking , Flexible memory

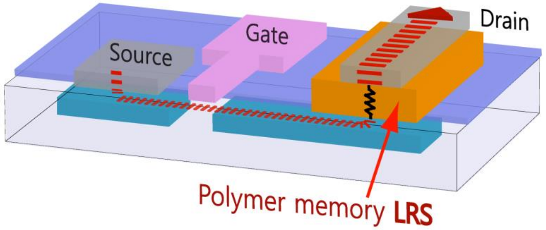
MIM



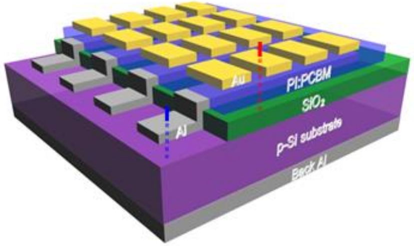
Cross bar



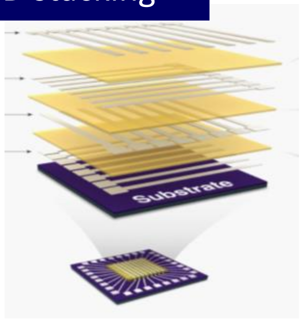
1T-1R



1D-1R

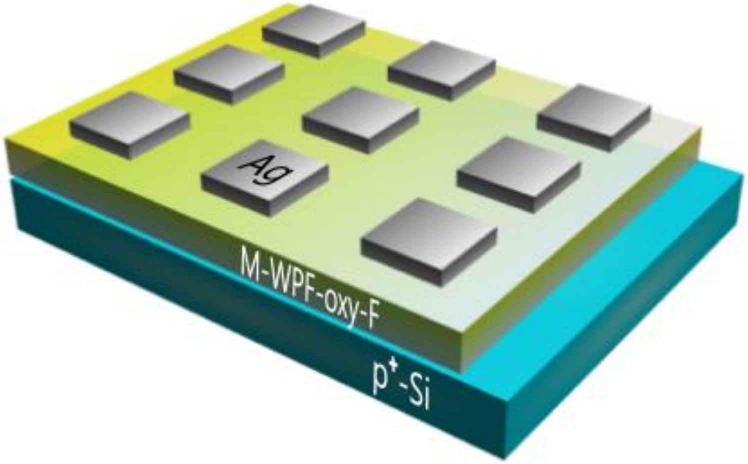


3D stacking



Flexible memory

Simple Architecture for Organic Non-volatile Memory

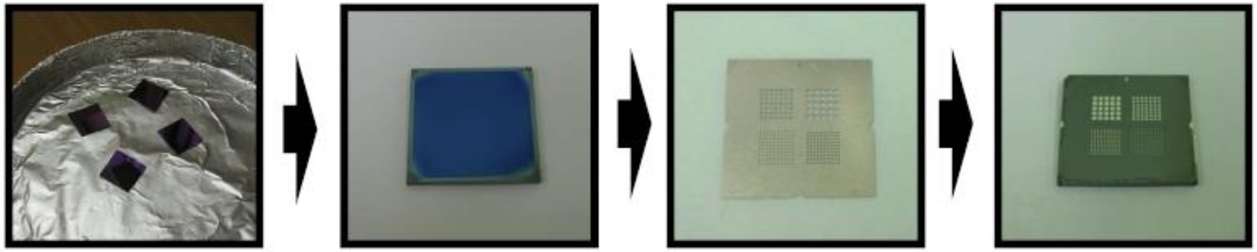


Kim *et al*. Applied Physics Letters 92, 253308 (2008)
Kim *et al*. IEEE Electron Device Letters 29, 852 (2008)
Kim *et al*. Nanotechnology 20, 025201 (2009)
Kim *et al*. Organic Electronics 10, 496 (2009)
Kim *et al*. Organic Electronics, 11, 109 (2010)
Cha *et al*. Materials Science and Engineering B, 191 (2015)
Cha *et al*. ACS Applied Materials & Interfaces, 9, 2730 (2017)

Simple Architecture for Organic Non-volatile Memory

M-I-M Unit-cell Type Single Layer Organic Memory Devices

Fabrication of polymer non-volatile memory device



Standard cleaning : Heavily doped P-type silicon

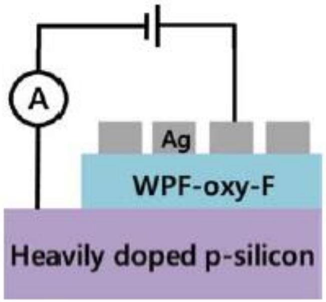
Spin coating of organic material & baking

Concentration: 5 mg/ml

2000rpm, 30s / 150°C, 20min

Formation of top electrode using shadow mask : M-I-M type

Top electrode deposition : M-I-M type



Cell size: 50, 100, 200, 400 μm

Equipment for fabrication and analysis

Glove Box

E-beam evaporator

Thermal evaporator

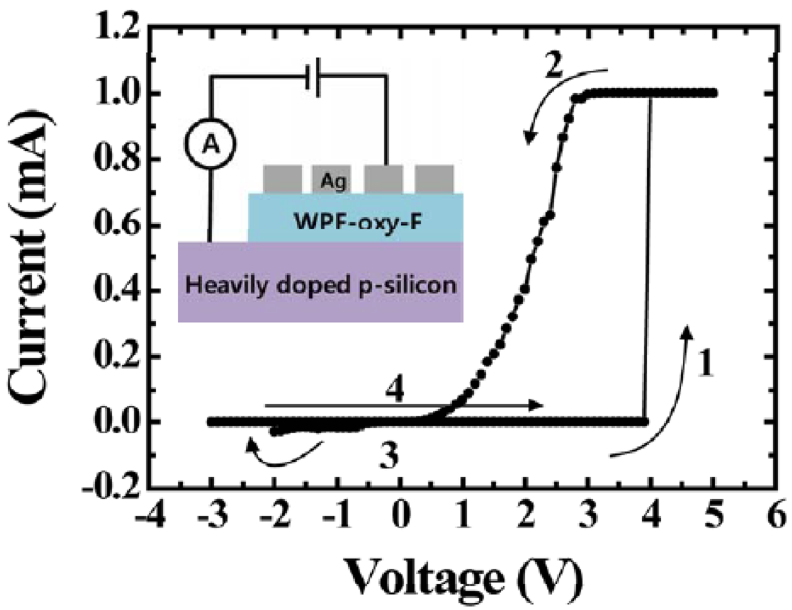
Conducting AFM

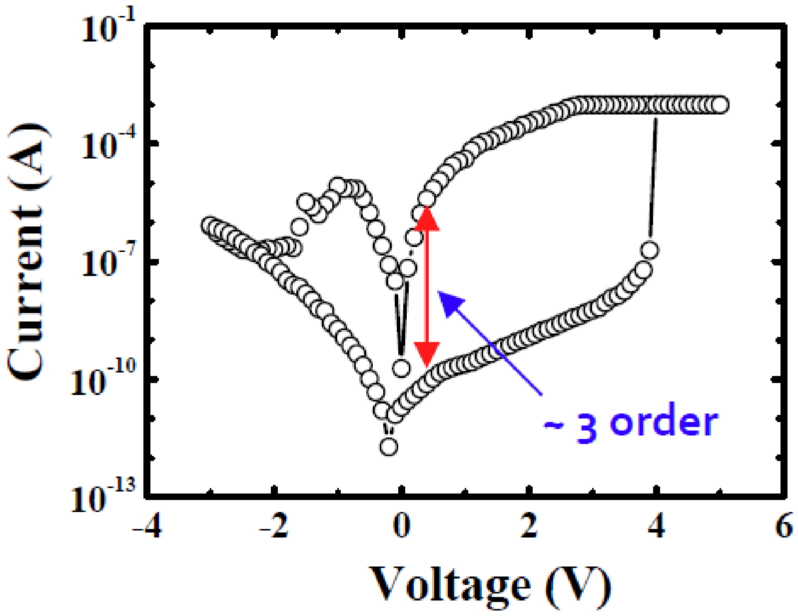
HP4155C, B1500A & Prove Station

HP4145B with Labview system

Simple Architecture for Organic Non-volatile Memory

Switching behavior of WPF-oxy-F memory devices





- WPF-oxy-F memory device showed bipolar switching behavior
- More than 3 orders of magnitude of on/off ratio
- Low operation voltage (-3V ~ 5V)

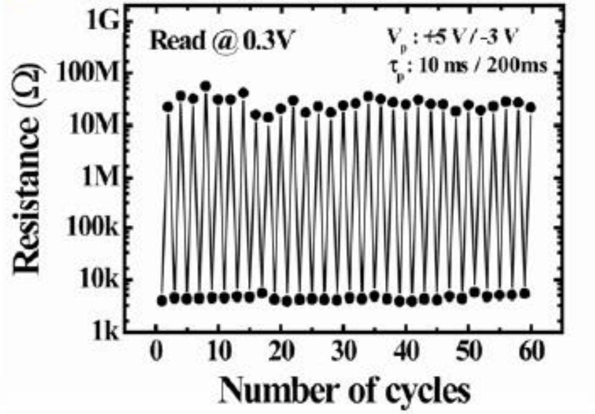
Kim *et al*, ***Appl. Phys. Lett.*** 92, 253308 (2008)
Kim *et al*, ***IEEE Electron. Device Lett.*** 29, 852 (2008)

I. Simple **architecture for organic memory device**

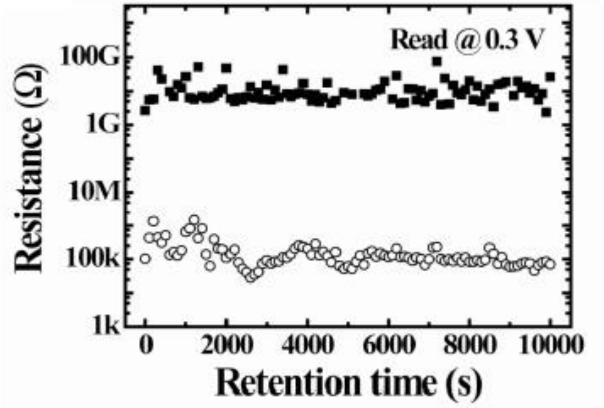
Micron-scale MIM / Submicron-scale MIM

Specific memory performances

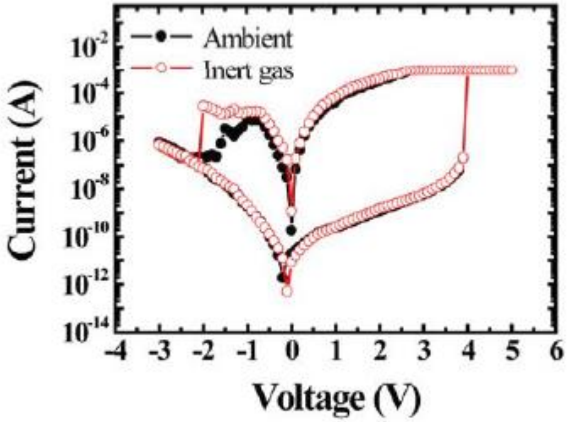
Cycling (pulsed I-V)



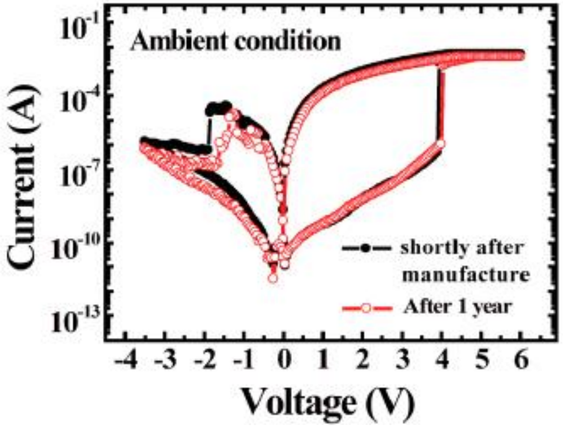
Retention characteristics



Ambient, inert environment



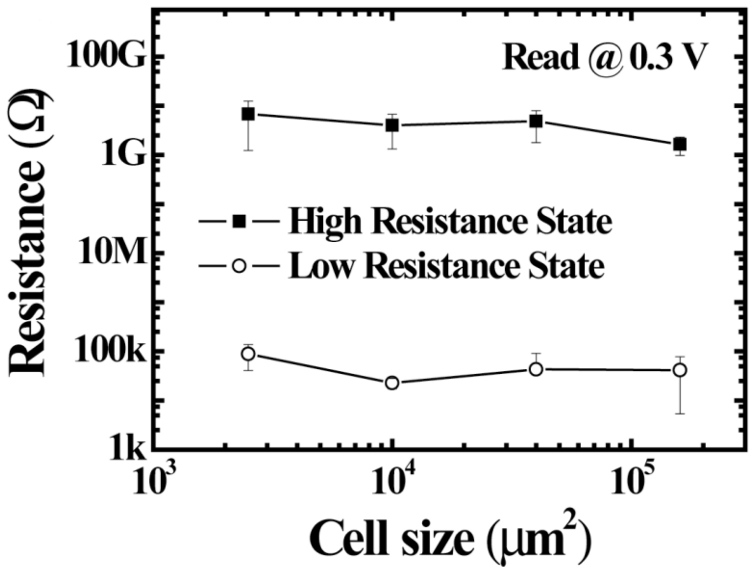
Stability



Simple Architecture for Organic Non-volatile Memory

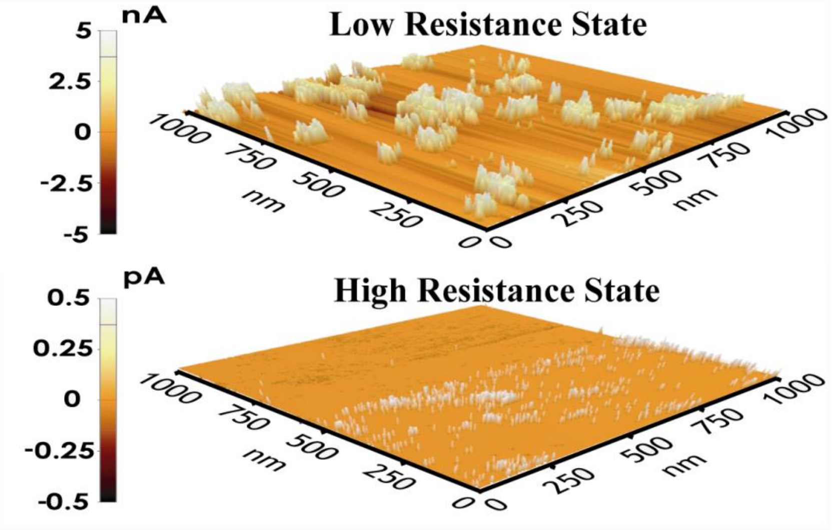
Memory Mechanism

Cell area dependence



- From ~120 devices for 50, 100, 200, 400 μm cell sizes
- Resistance of LRS did not change over cell size
- Resistance of HRS slightly decreased

Conducting-AFM images



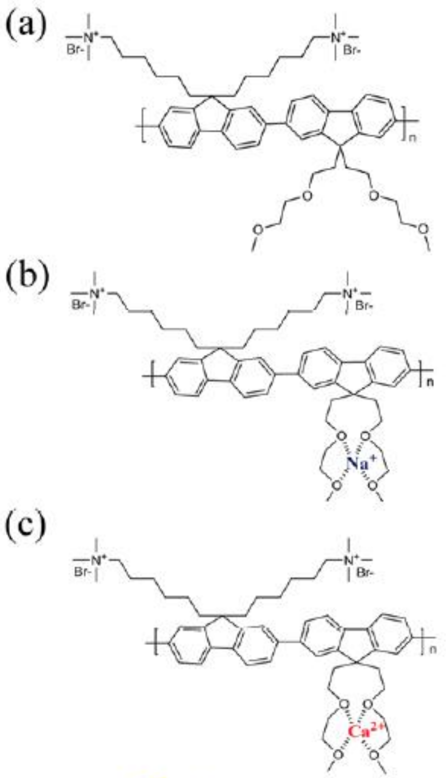
There are localized and distributed conduction paths in current image of LRS

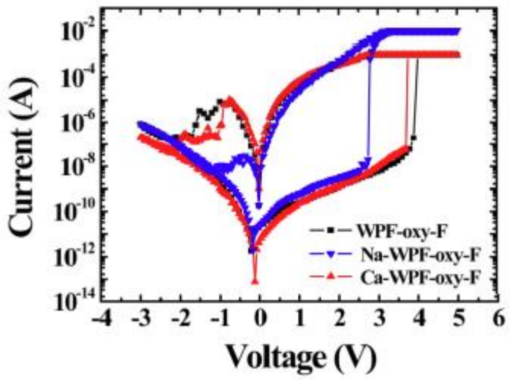
Programming : 6.5V tip bias
Erasing : -3.0V tip bias
Reading : 1.0V tip bias

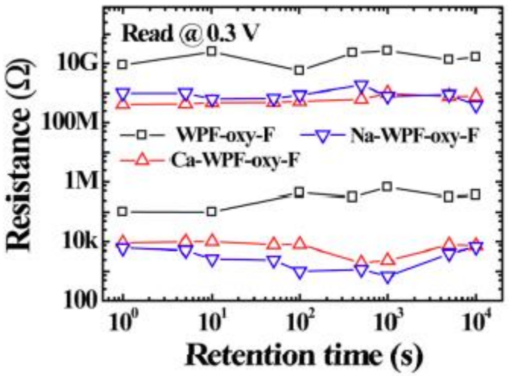
Kim *et al*, ***Appl. Phys. Lett.*** 92, 253308 (**2008**)

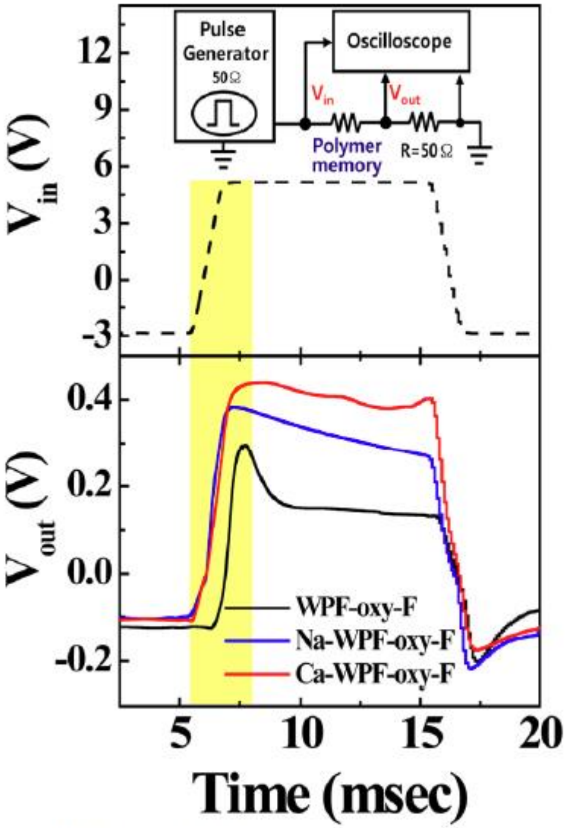
Simple Architecture for Organic Non-volatile Memory

Switching (Response) Time







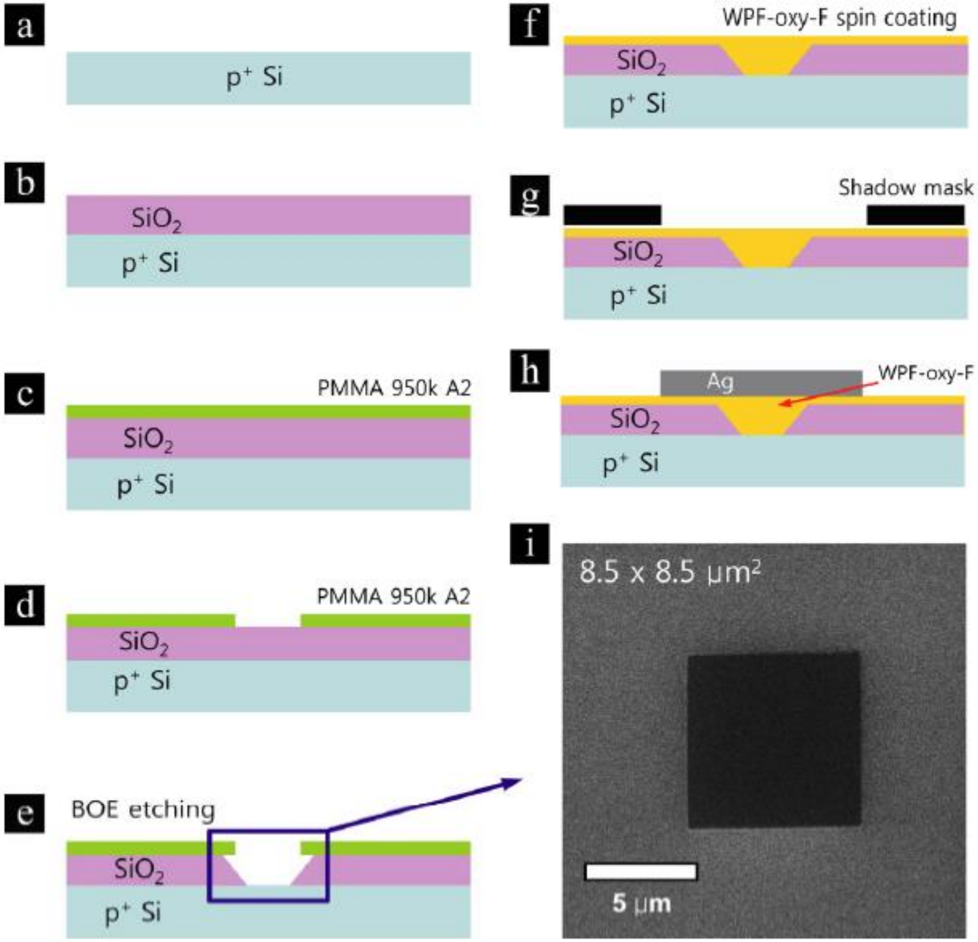


- Response time when switching from HRS to LRS:
  Na-WPF-oxy-F and Ca-WPF-oxy-F: ~10 μs
  WPF-oxy-F: ~2 ms

Kim et al. Organic Elect. 10, 496 (2009)

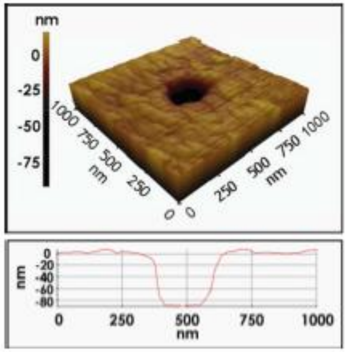
Sub-micron scale Organic Non-volatile Memory

Nanoscale (Sub-micron scale) M-I-M Unit-cell Devices



- E- Beam lithography technique
- Wet etching process (BOE)
- Size of via-hole

$40 \times 40\ \mu m^2$
$8.5 \times 8.5\ \mu m^2$
$4.5 \times 4.5\ \mu m^2$
$1 \times 1\ \mu m^2$
$500 \times 500\ nm^2$
$200 \times 200\ nm^2$

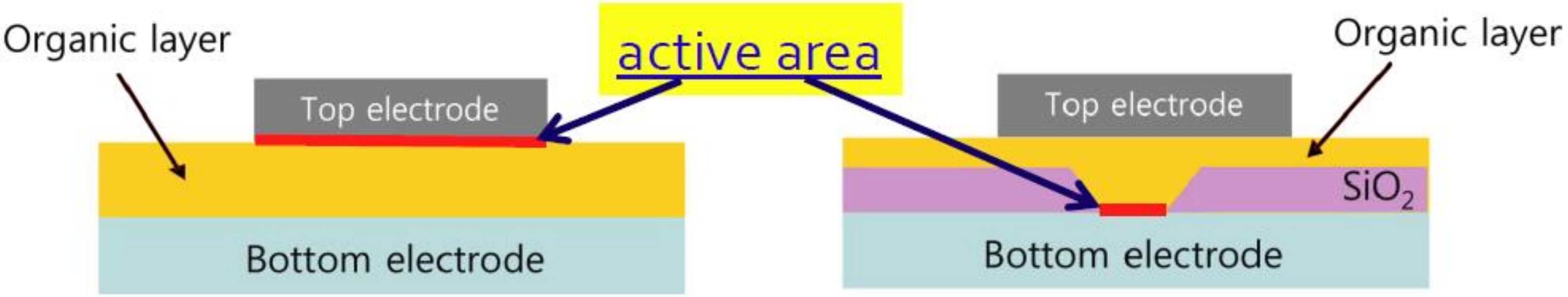


Kim et al. Nanotechnology, 20, 025201 (2009)

Sub-micron scale Organic Non-volatile Memory

What is the difference between *conventional M-I-M* between *scalable via-hole* ?

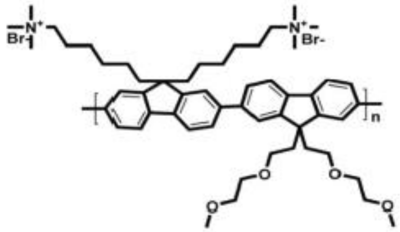
- **Conventional MIM**
- **Scalable via-hole**



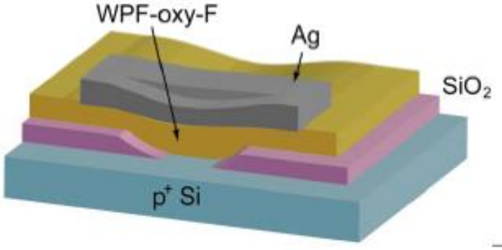
➡ The main difference is how to define active area.

In this study

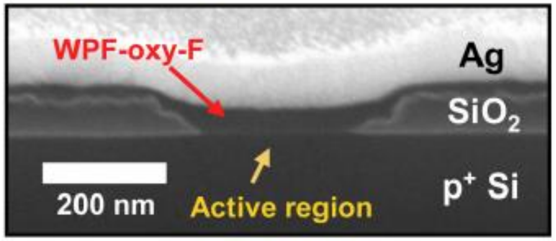
- Organic material



- 3D schematics



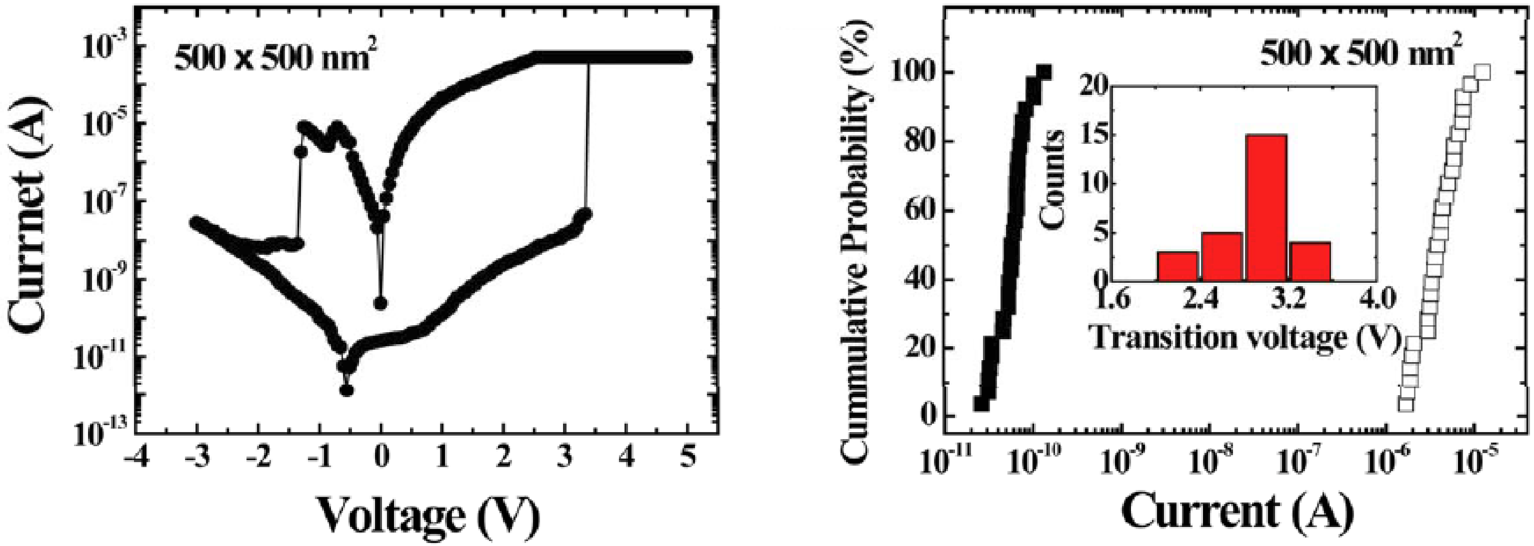
- SEM image of organic memory device



Sub-micron scale Organic Non-volatile Memory

Nanoscale (Sub-micron scale) switching characteristics

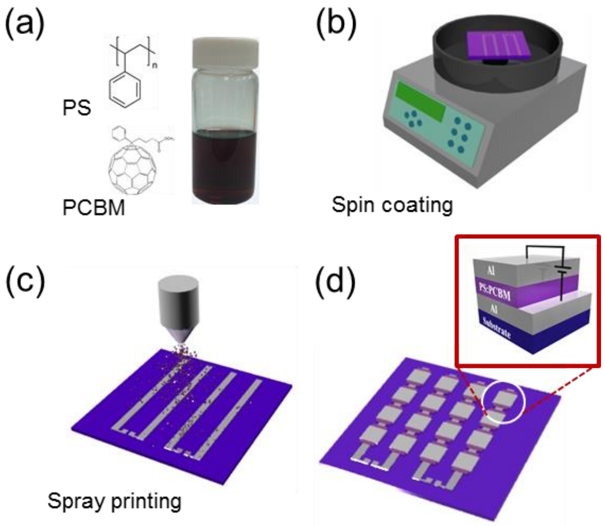
Switching behavior of sub-micron scale polymer memory device



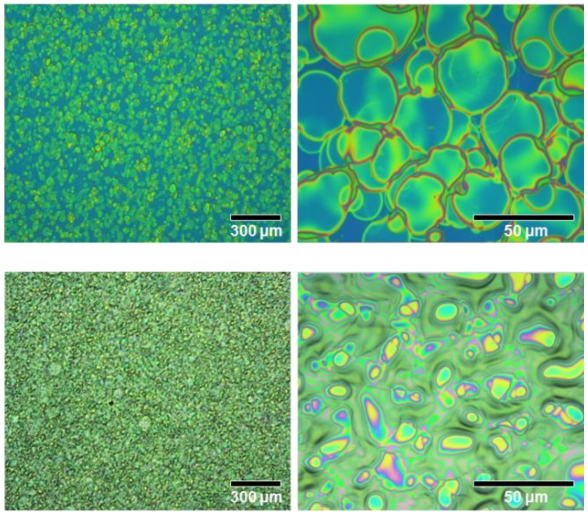
- Excellent electrical bistability with a high ON/OFF ratio (I_{ON}/I_{OFF} ~10^4 at 0.3 V)
- Excellent device-to-device switching uniformity
- Narrow distribution of transition voltage (2.8V ~ 3.2 V)

Organic Non-volatile Memory by Printing Process

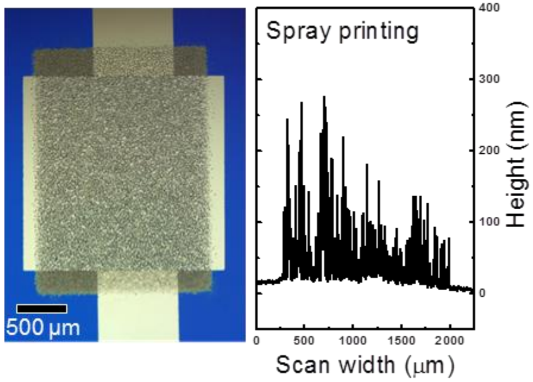
- Organic memory devices via. spray printing method



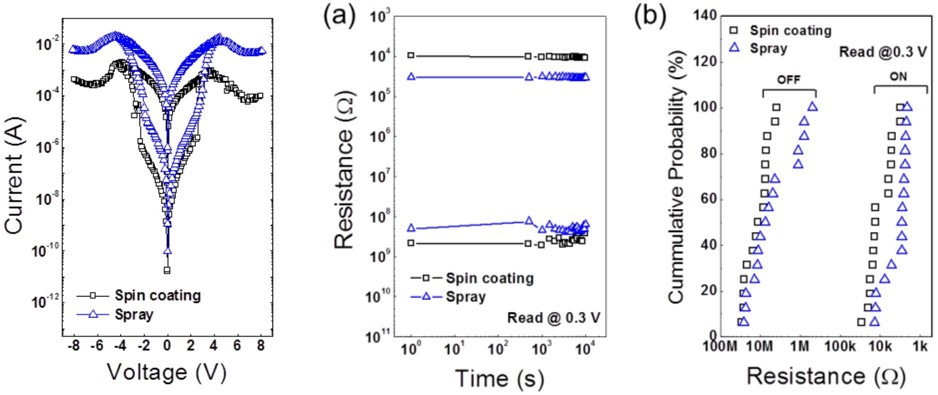
Optical images of sprayed film



Optical image



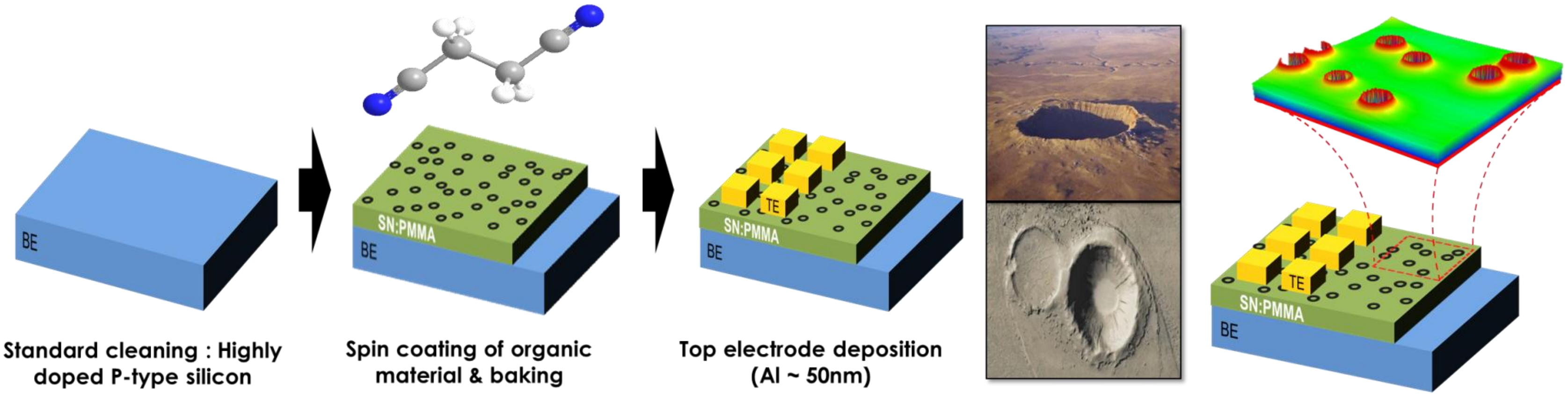
Electrical properties



Cha *et al.* Materials Science and Engineering B, 191 (2015)

Self-assembled Organic Composite Non-volatile Memory

- Micro-crater from succinonitile-poly(methyl methacrylate) organic composite



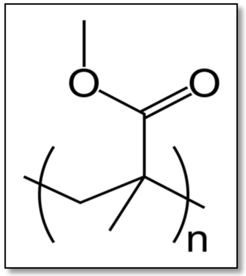
Standard cleaning : Highly doped P-type silicon

Spin coating of organic material & baking

Top electrode deposition (Al ~ 50nm)

▶ Active layer (PMMA:SN) is polystyrene in chlorobenzene Spin casting was performed under 2000rpm for 40sec.

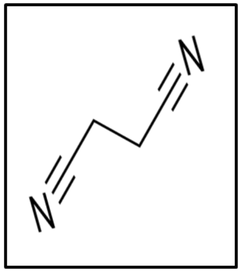
Poly(methyl methacrylate)



- Density 1.18 g/cm3
- Electrical conductivity (s) 10−19 S/m
- Thermal conductivity (k) 0.19 W/(m ·K)
- Melting point 160 °C
- Specific heat (c) 1.4 kJ/(kg ·K)

- **Poly(methyl methacrylate) (PMMA)** is a transparent thermoplastic often used in sheet form as a lightweight or shatter-resistant alternative to soda-lime glass.
- The same material can be utilised as a casting resin; in inks and coatings, and also has other uses.

Succinonitile



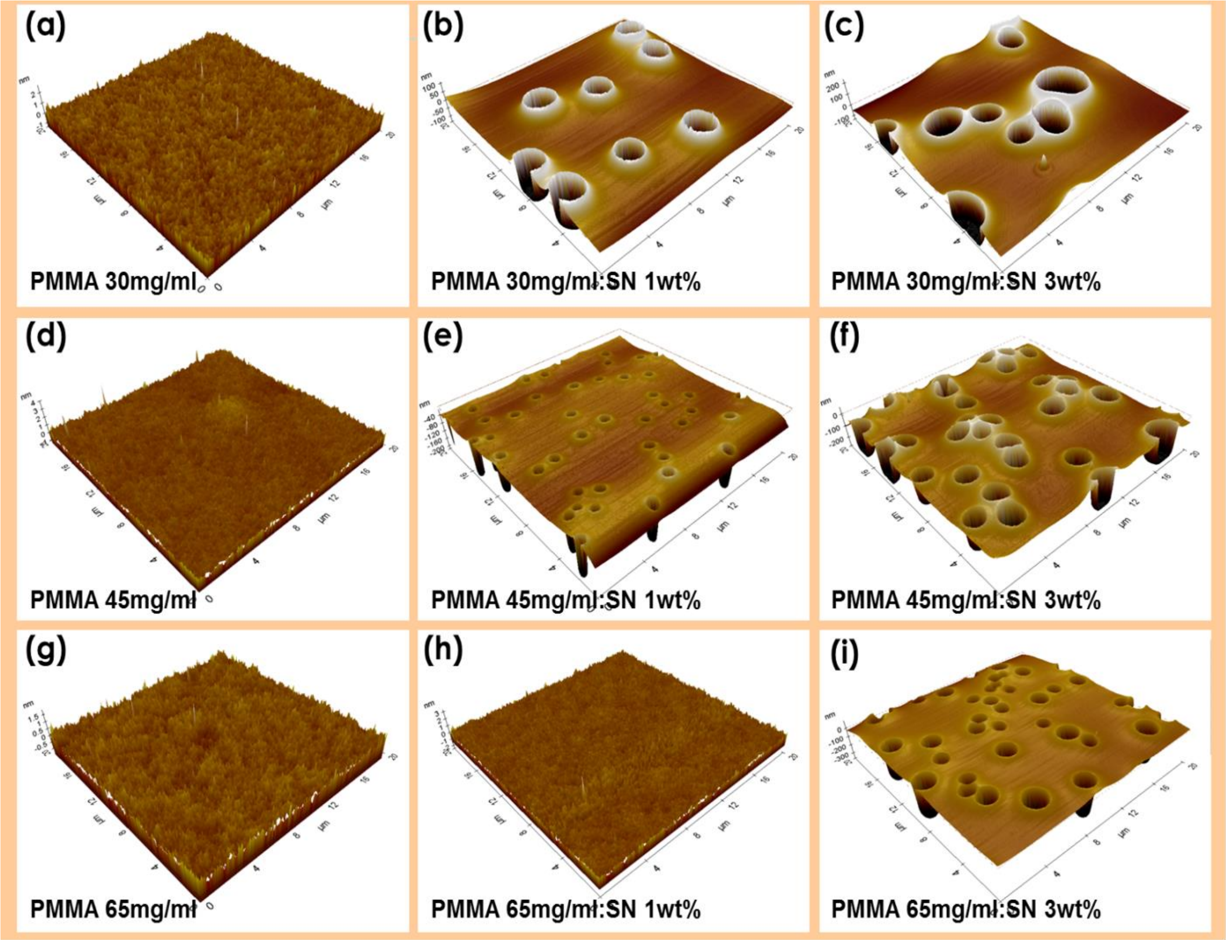
- Density 985 mg mL^{-1}
- Melting point 52 °C
- Specific heat (c) 145.60 J K^{-1} mol^{-1}

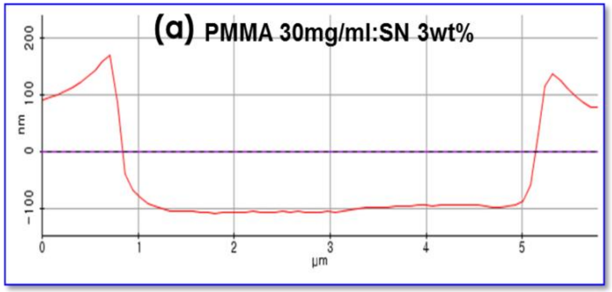
- **Succinonitrile**, also butanedinitrile, is a nitrile, with the formula of $C_2H_4(CN)_2$. It is a colorless solid that melts at 57 °C, hence its waxy consistency.

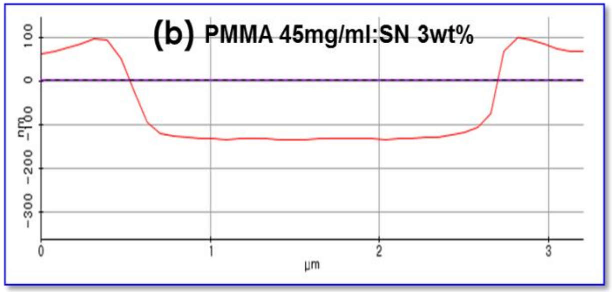
Cha *et al*. ACS Applied Materials & Interfaces, 9, 2730 (2017)

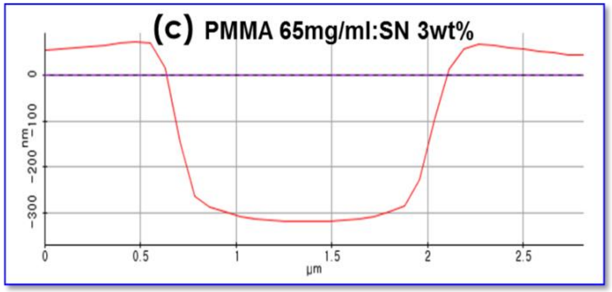
Self-assembled Organic Composite Non-volatile Memory

- AFM images of PMMA:SN composite film





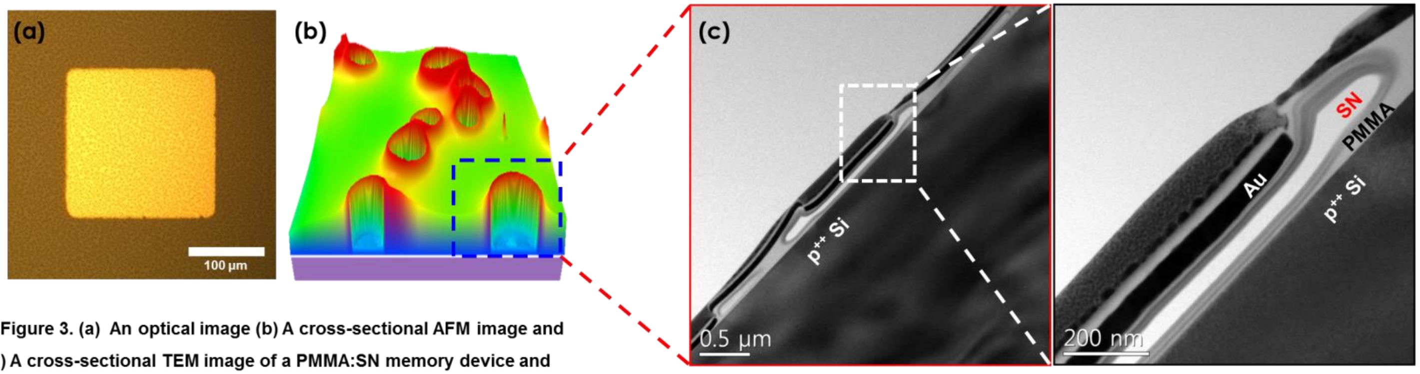




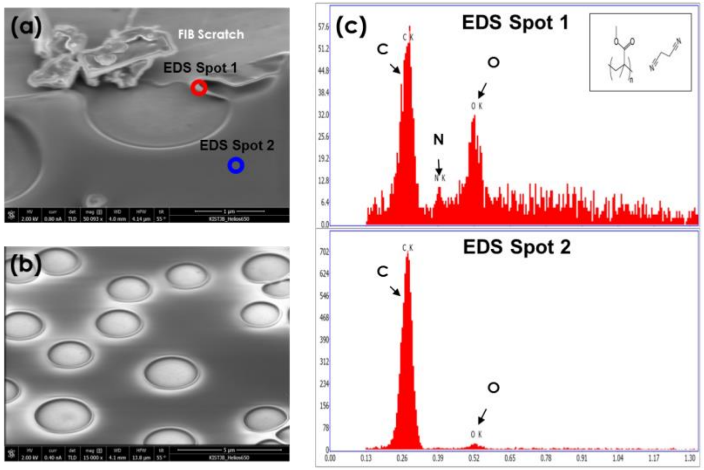
Self-assembled Organic Composite Non-volatile Memory

- TEM, EDX, XPS analysis on PMMA:SN composite film

  - **Optical microscopy images of organic non-volatile memory device with spin-coating process**



- Figure 3. (a) An optical image (b) A cross-sectional AFM image and (c) A cross-sectional TEM image of a PMMA:SN memory device and HRTEM image an PMMA:SN film memory device.



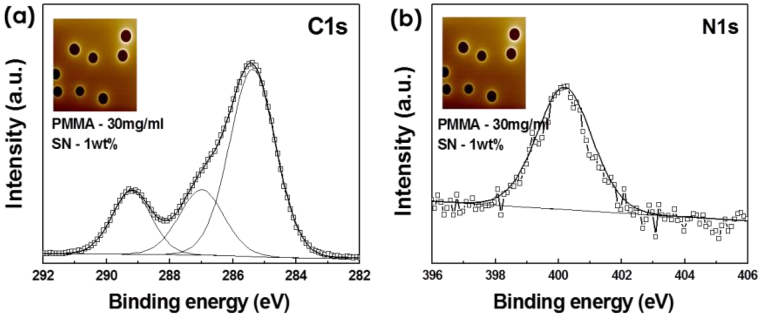
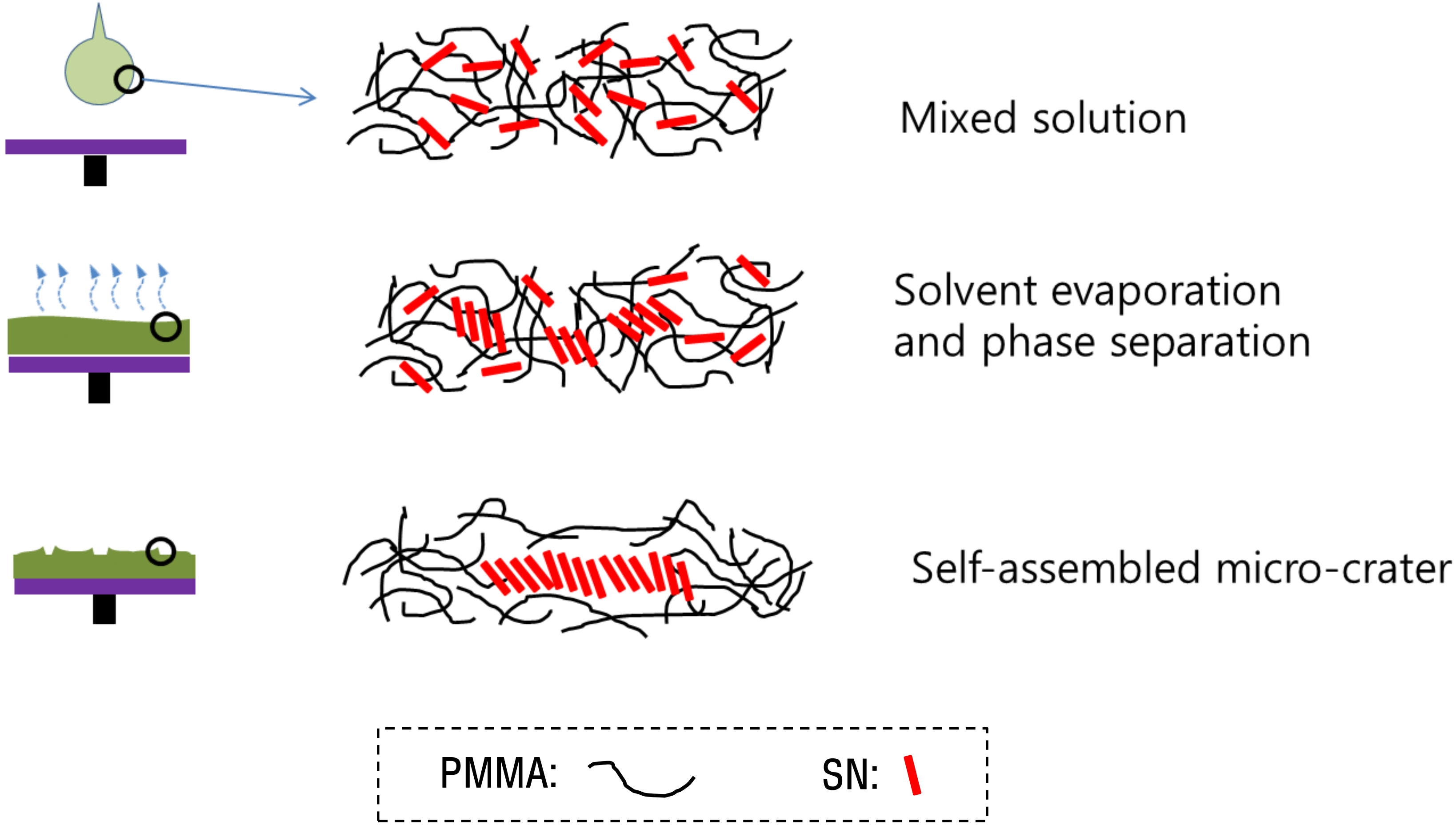


Figure 5. In situ XPS spectra of (a) C 1s and (b) N 1S regions measured as a function of PMMA 30mg/ml SN 1wt%.

PMMA:CB	SN 0 wt%	SN 1 wt%	SN 3 wt%
65mg/ml	~308nm	~305nm	~300nm
45mg/ml	~165nm	~160nm	~158nm
30mg/ml	~108nm	~103nm	~105nm

Self-assembled Organic Composite Non-volatile Memory

- Formation of micro craters



Mixed solution

Solvent evaporation and phase separation

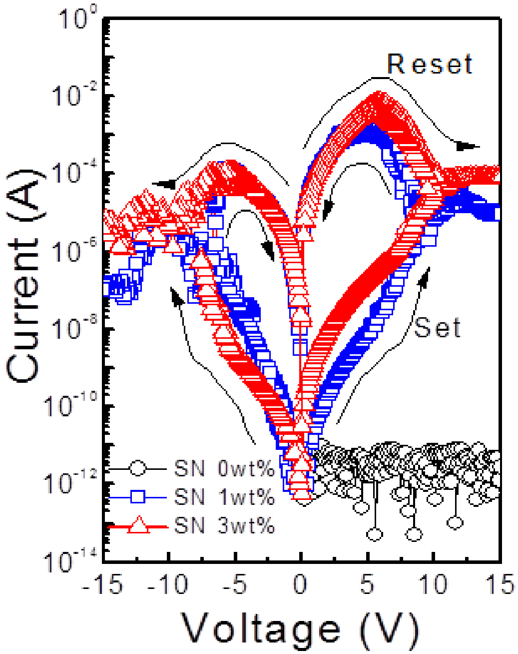
Self-assembled micro-crater

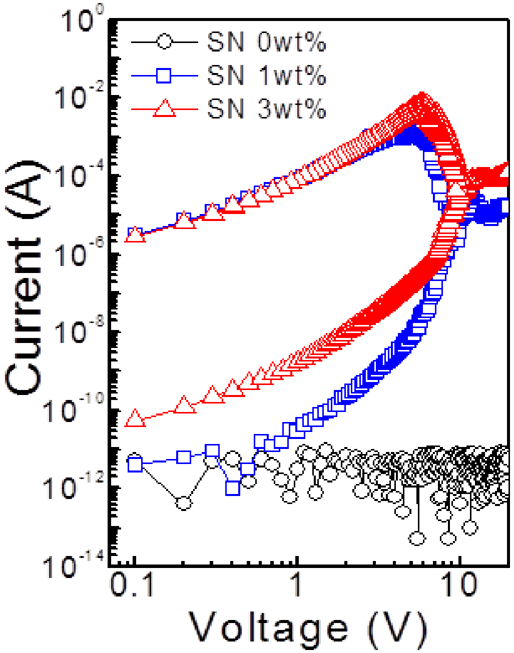
PMMA: 〰

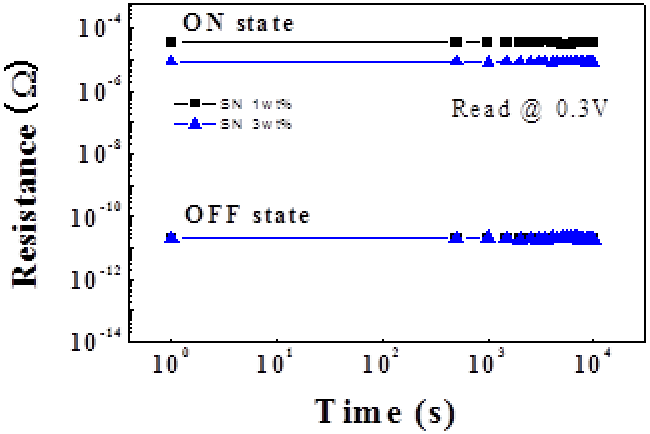
SN: ▮

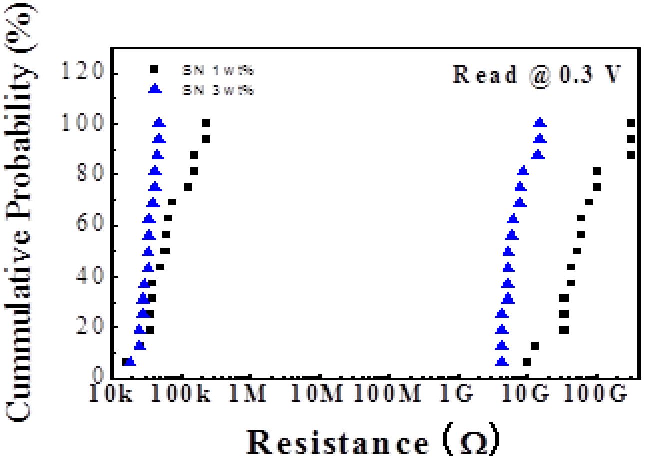
Self-assembled Organic Composite Non-volatile Memory

- Electrical properties of PMMA:SN composite film



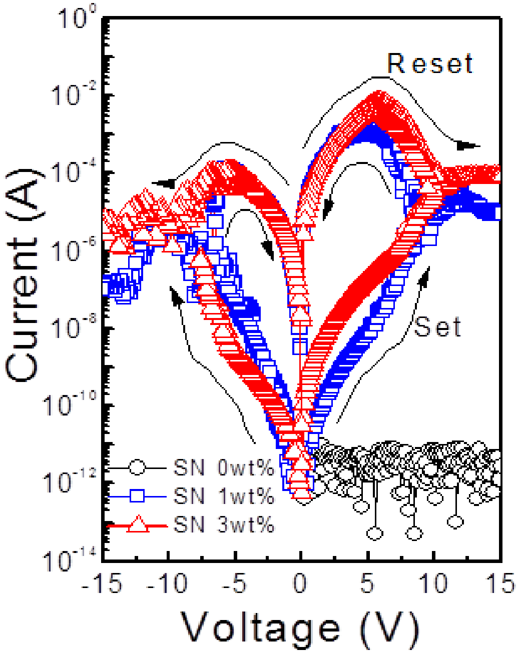


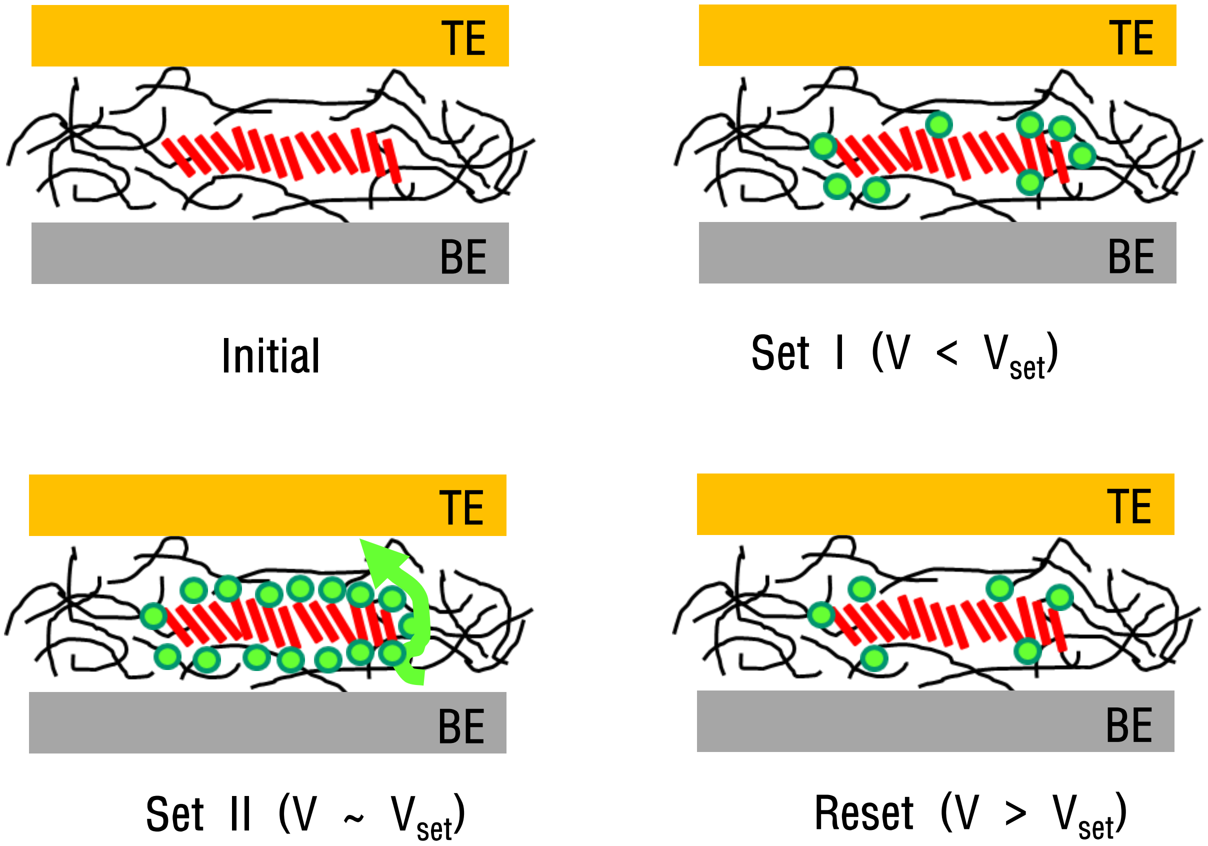


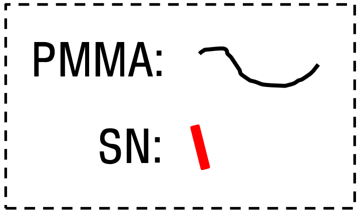


Self-assembled Organic Composite Non-volatile Memory

- Potential switching mechanism

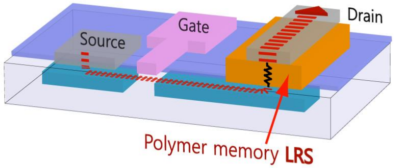


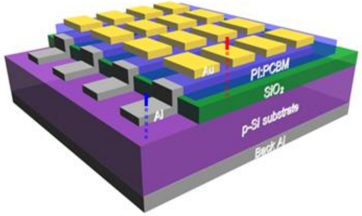


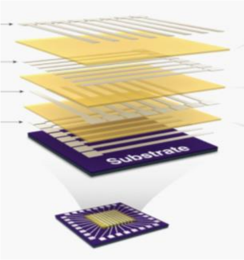


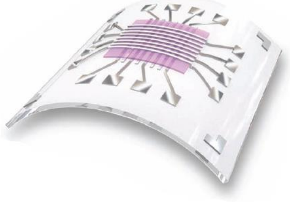
Cha *et al*. ACS Applied Materials & Interfaces, 9, 2730 (2017)

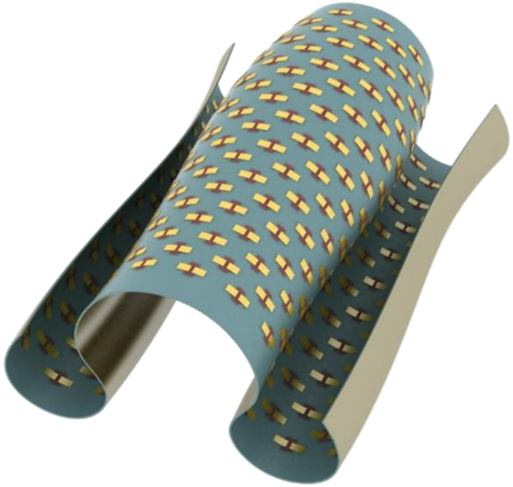
Advanced Architecture for Organic Non-volatile Memory

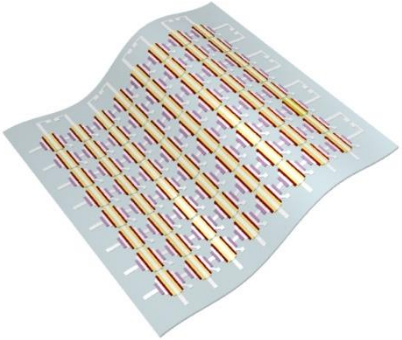


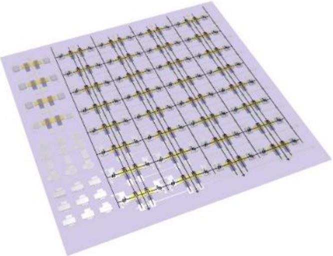


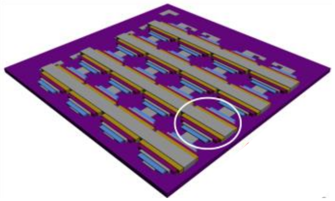








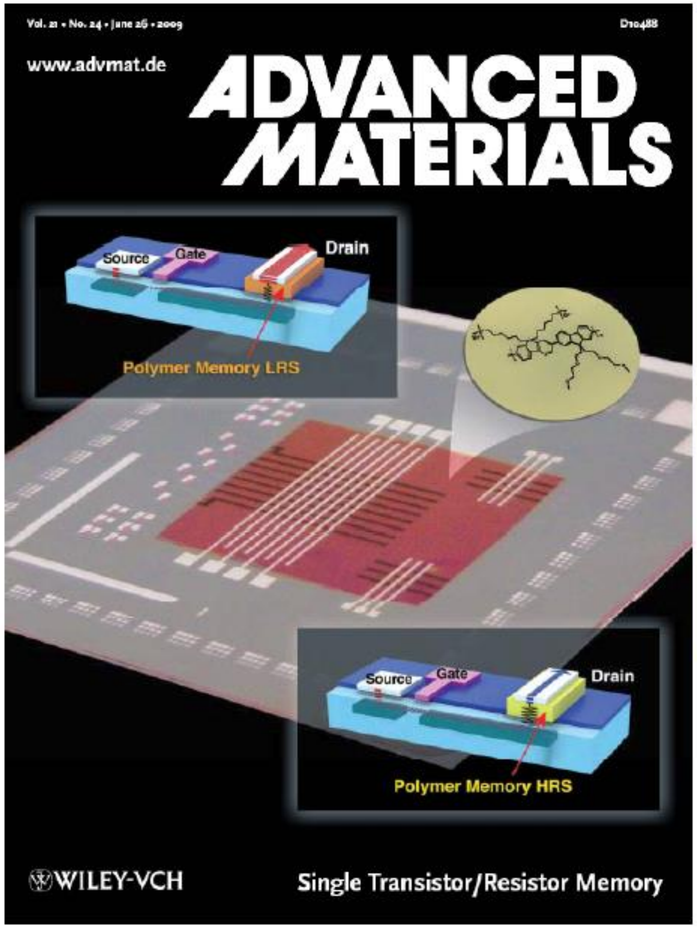


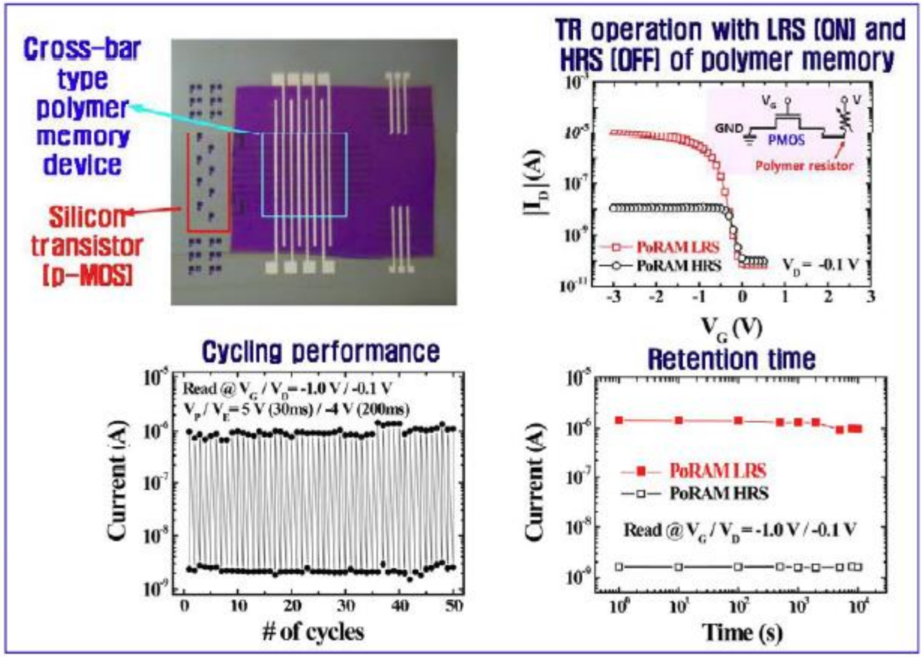


Kim *et al*. Advanced Materials, 21, 2497 (2009)
Cho, Kim *et al*. Advanced Materials, 22, 1228 (2010)
Ji, Kim *et al*. Advanced Materials, 22, 3071 (2010)
Song, Kim *et al*. Advanced Materials, 22, 5048 (2010)
Kim *et al*. Advanced Materials, 24, 828 (2012)
Ji *et al*, Nature Communications, 4:2707 (2013)
Ji *et al*, Organic Electronics, 18, 77 (2015)
Ji *et al,* Organic Electronics, 29, 66-71 (2016)
Jang *et al*, In Revision (2018)

Advanced Architecture for Organic Non-volatile Memory

- 1T-1R Organic Memory Device

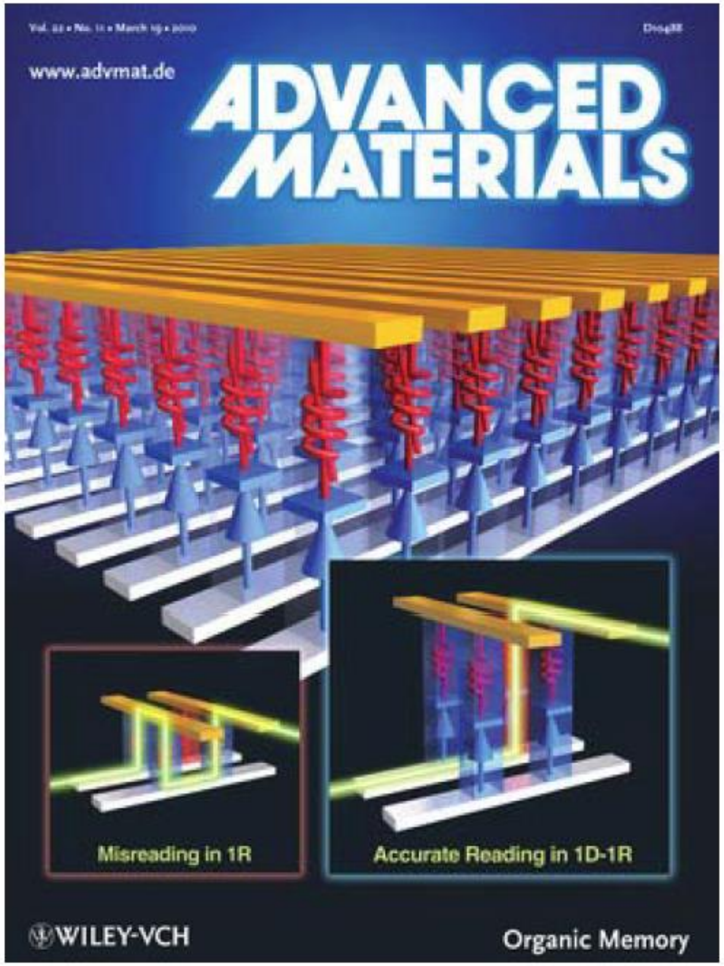


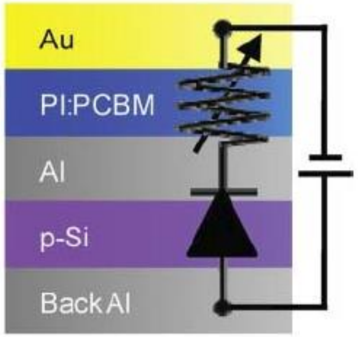


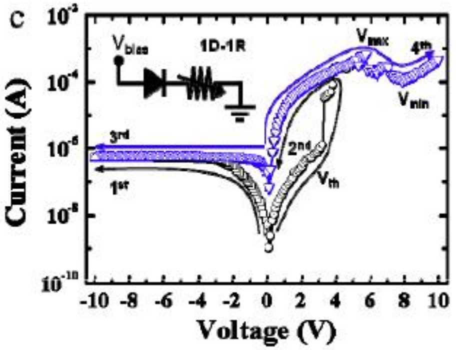
Kim *et al*. Advanced Materials, 21, 2497 (2009)
COVER

Advanced Architecture for Organic Non-volatile Memory

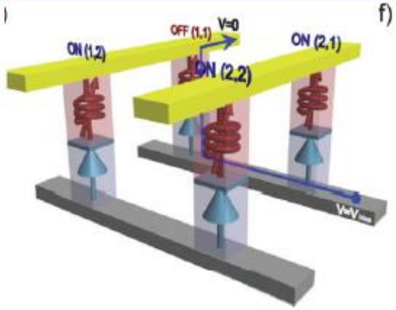
- 1D-1R Organic Memory Device







❖Accurate reading process in 1D-1R array



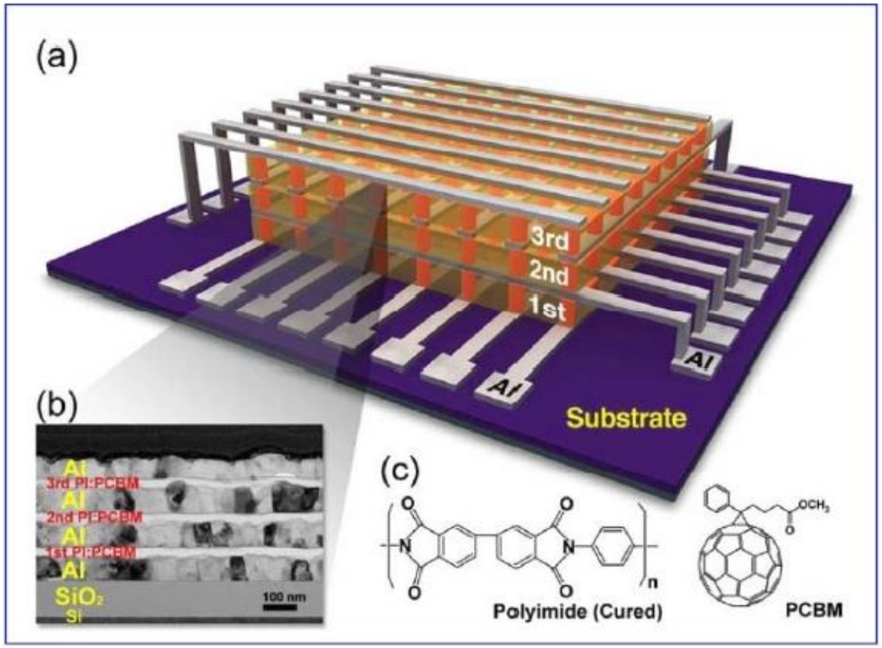
Resistance (Ω) in 1D1R		
W/L B/L	1	2
1	4.2 M (OFF)	27.3 K (ON)
2	24 K (ON)	16.3 K (ON)

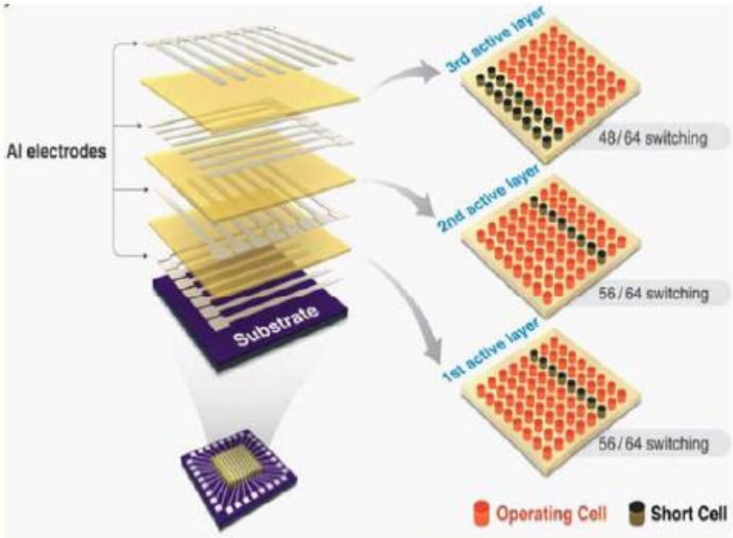
Cho, Kim *et al*. Advanced Materials, 22, 1228 (2010)

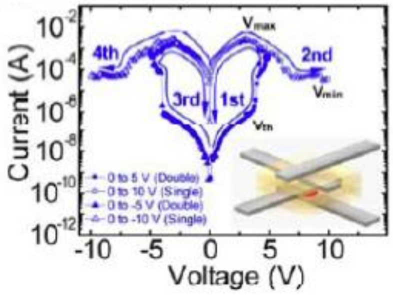
COVER

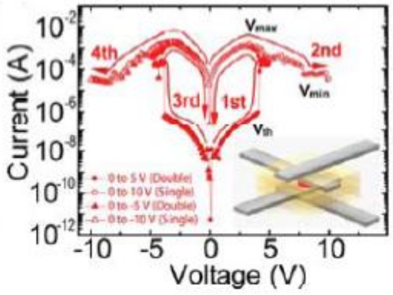
Advanced Architecture for Organic Non-volatile Memory

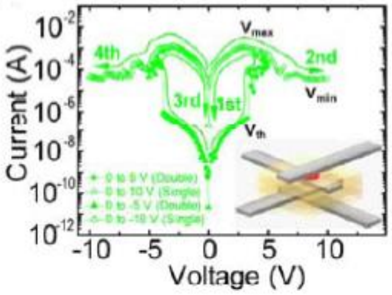
- 3-D Integrated Organic Non-volatile Memory Cell Array

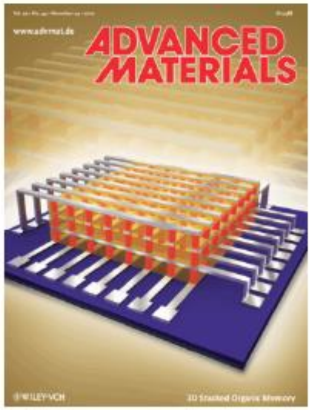










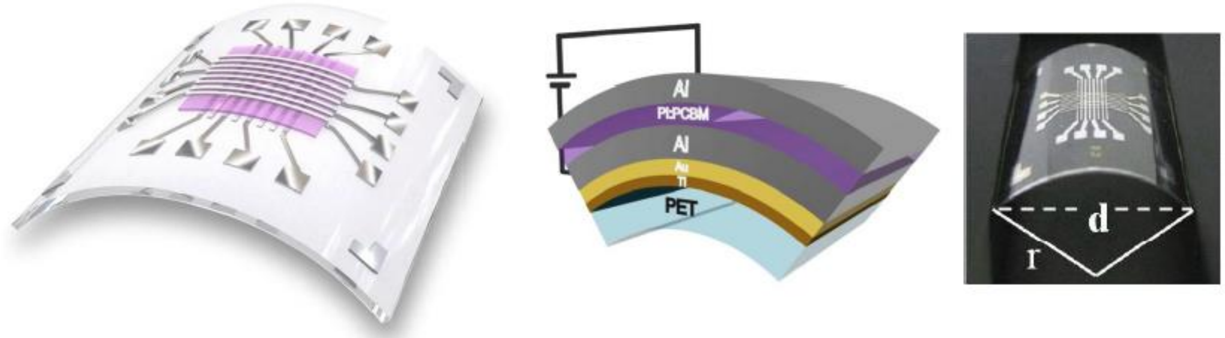


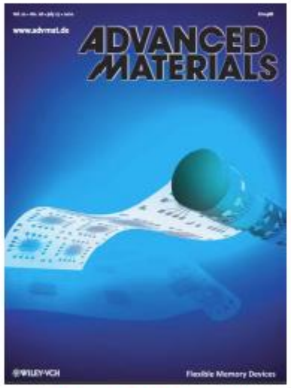
Song, Kim *et al*. Advanced Materials, 22, 5048 (2010)

Advanced Architecture for Organic Non-volatile Memory

- Flexible Organic Non-volatile Memory

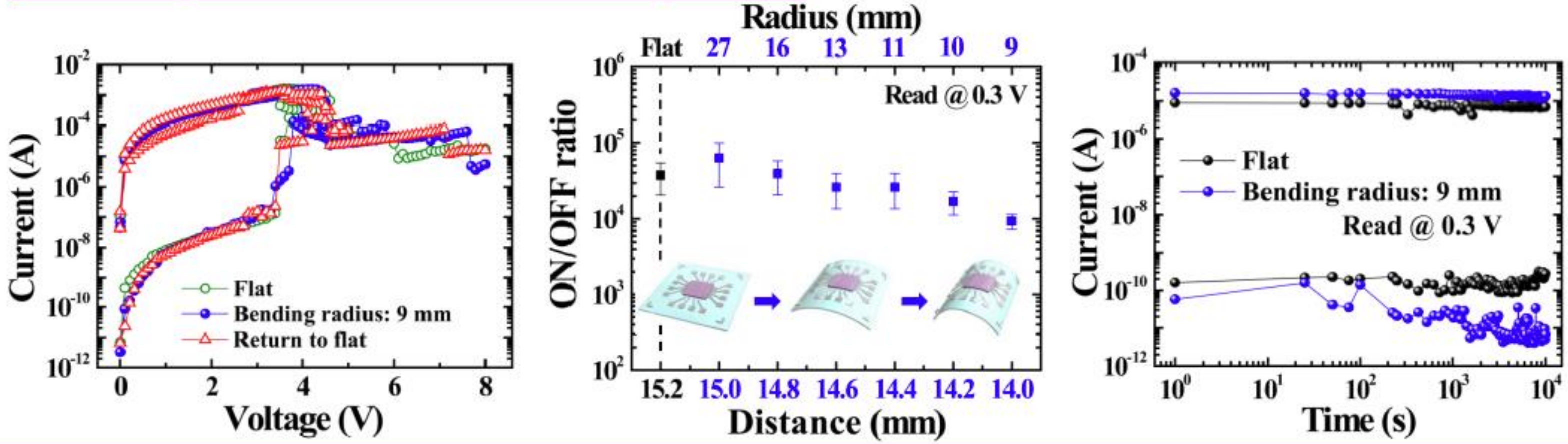
❖Flexible organic memory device





Front Cover

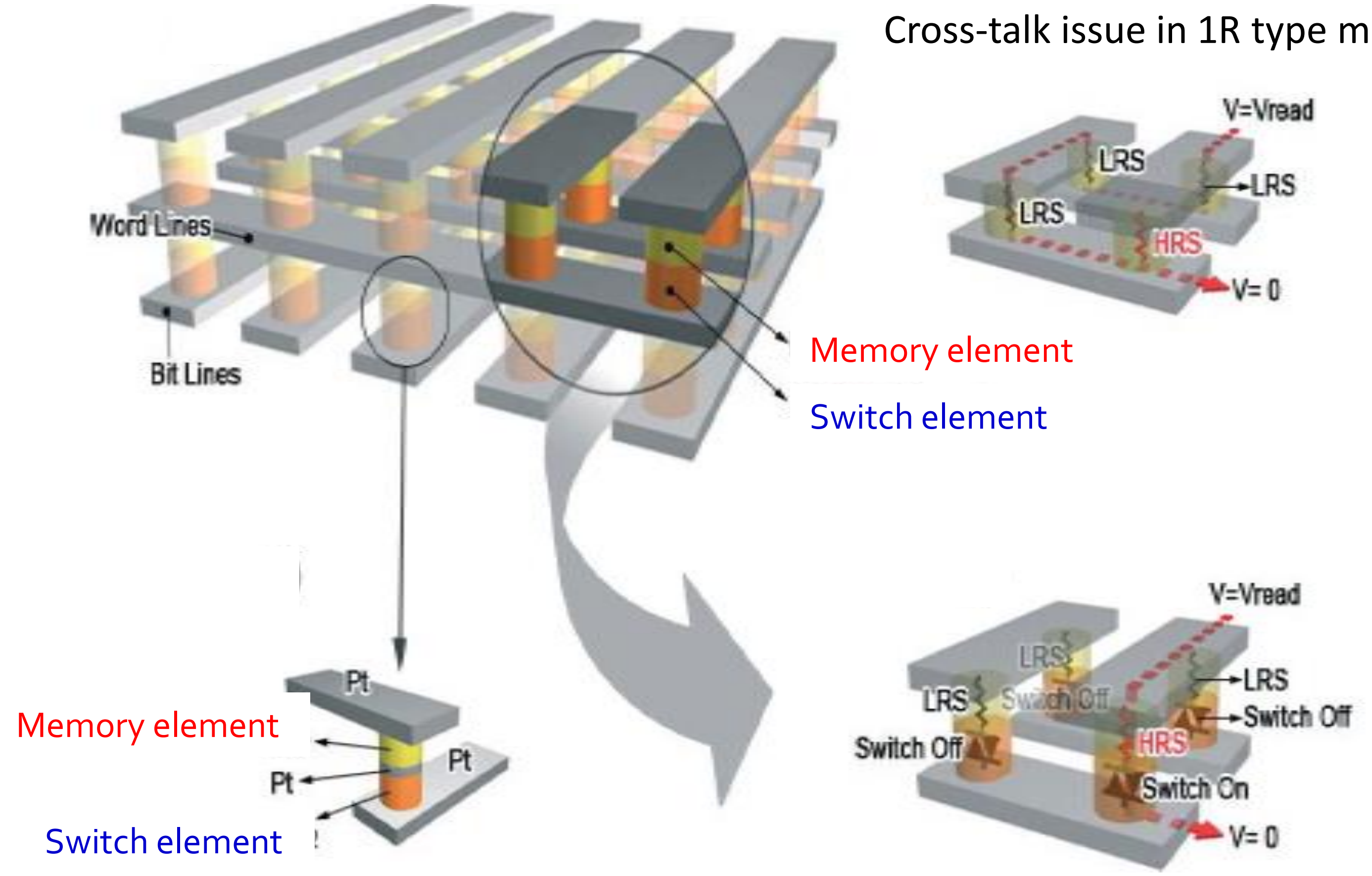
❖Switching characteristics of flexible memory device



Ji, Kim *et al.* Advanced Materials, 22, 3071 (2010)

1D-1R Architecture for Organic Non-volatile Memory

- Why 1D-1R Architecture?



Cross-talk issue in 1R type memory cell array

Memory element

Switch element

Memory element

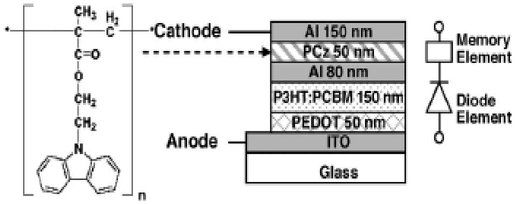
Switch element

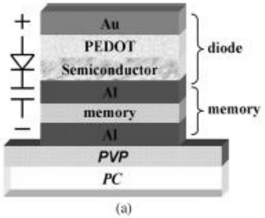
M.-J. Lee et al (Samsung), Adv. Func. Mater. (2007)

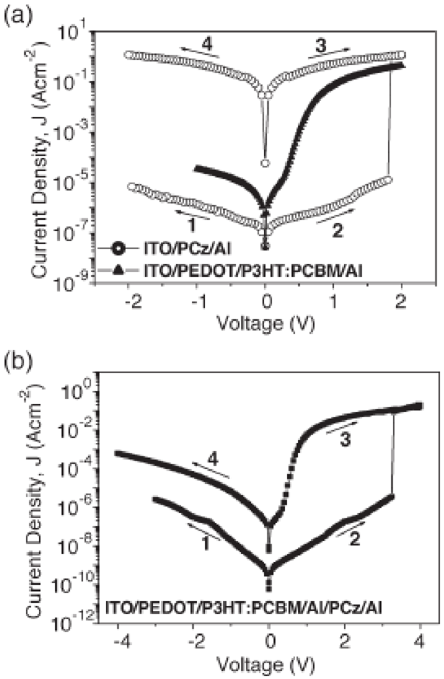
1D-1R Architecture for Organic Non-volatile Memory

- Recent researches on organic 1D-1R

All Organic 1D-1R but WORM type: No isolated cell



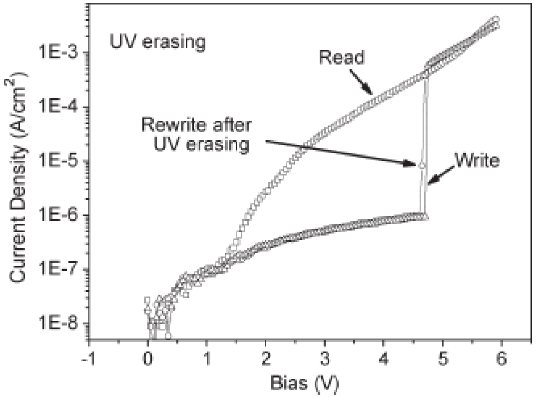




Teo *et al*, IEEE EDL, 30,489 (2009)

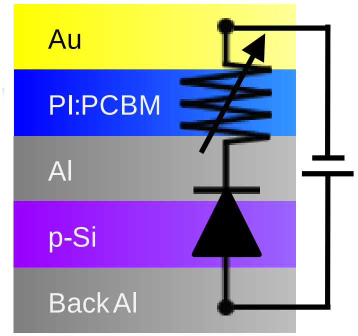
Memory layer: Gold nanoparticles (**Au-PCm**) with a size distribution of 3–5 nm are dissolved in a 4-Cyano-2,4,4-trimethyl-2-ethylsulfanylthiocarbonylsulfanyl- poly (butyric acid 1-adamantan- 1-yl-1-methyl-ethyl ester) (**PCm**)

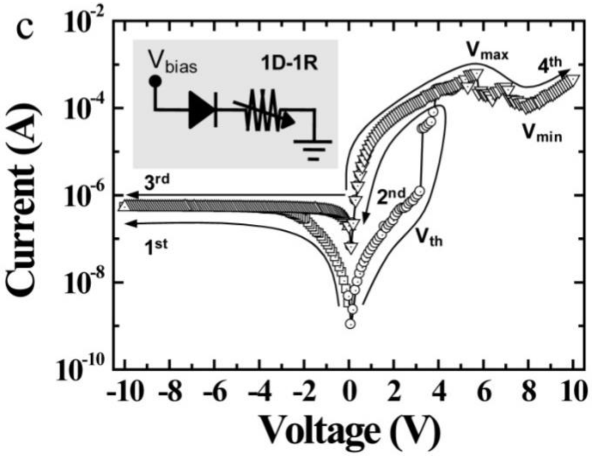
Diode layer: P3HT/PEDOT:PSS



Lin *et al*, IEEE EDL, 30,18 (2009)

hybrid 1D-1R: Rewritable





Cho, Kim *et al*, Advanced Materials, 22, 1228 (2010)

1D-1R Architecture for Organic Non-volatile Memory

- All organic patternable 1D-1R Organic Non-volatile memory cell array

Issues on organic memory device (resistive change type)

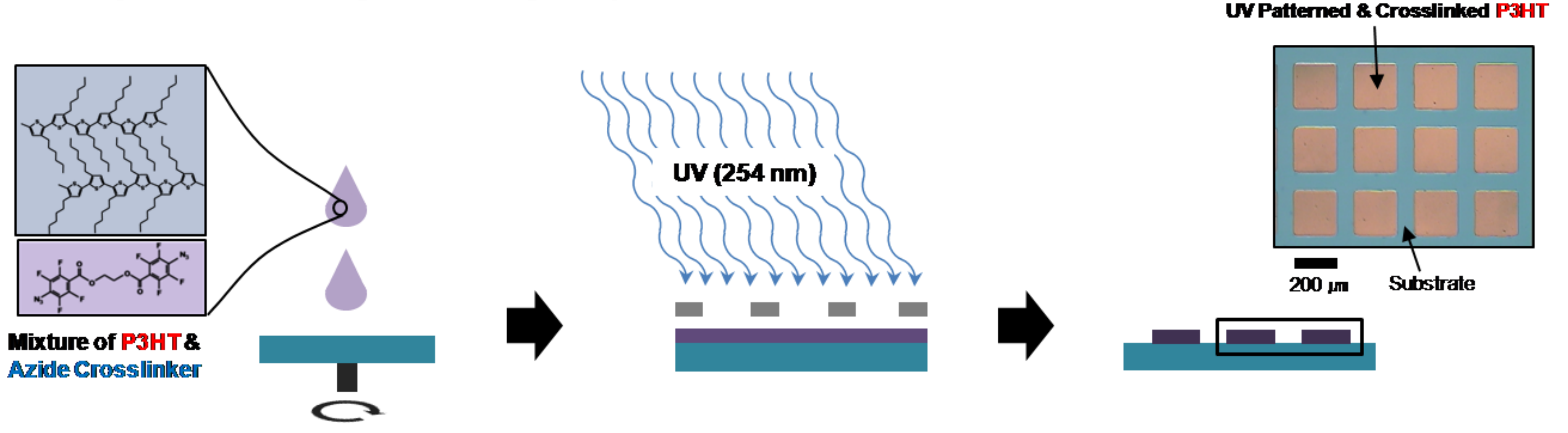
- **Processability**
- **How to Integrate**
- **Development of novel architecture**

Strategy to achieve better processability and device integration

➡ UV patterning & crosslinking for further process

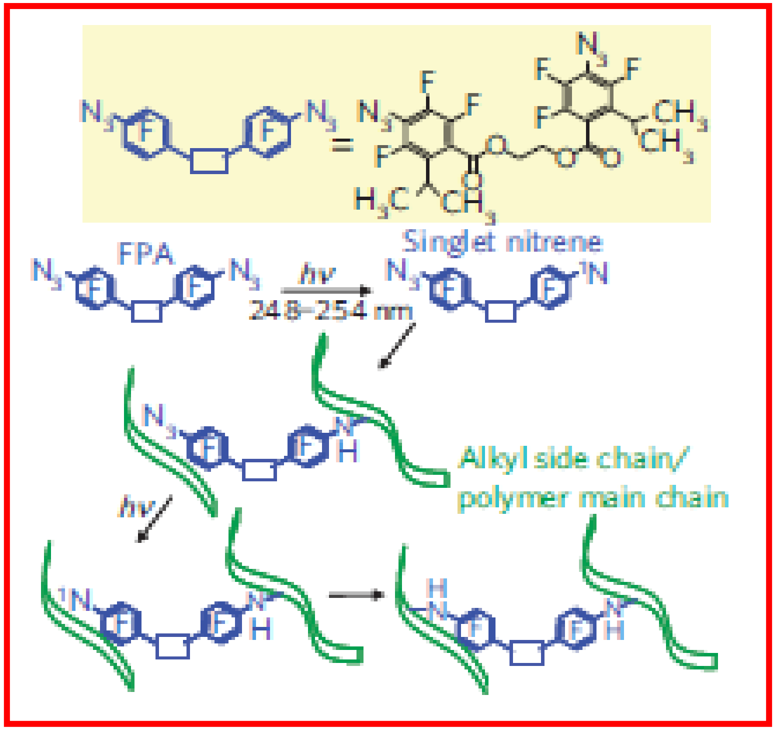
- Use of UV patternable polymer (**Memory component** : Resistor)
- Azide crosslinker for patterning of common conjugated polymers (**Switching Component**: Diode)

Example - UV Patterning of Switching Component



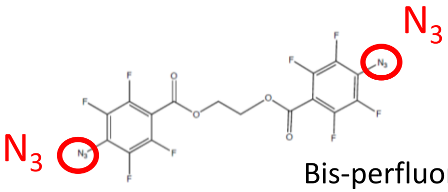
1D-1R Architecture for Organic Non-volatile Memory

Small molecule for cross linking of organic materials



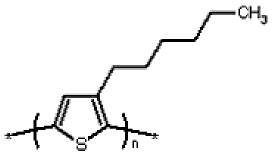
Bis(fluorophenyl azide)s (sFPAs) can be mixed generally into polymer OSCs to cause photocrosslinking when exposed to deep- ultraviolet light (DUV, 254nm wavelength) without degrading their essential semiconductor properties.

- Our Cross linker



Bis-perfluorobenzoazide (Bis-FB-N$_3$)

- p-type polymer material



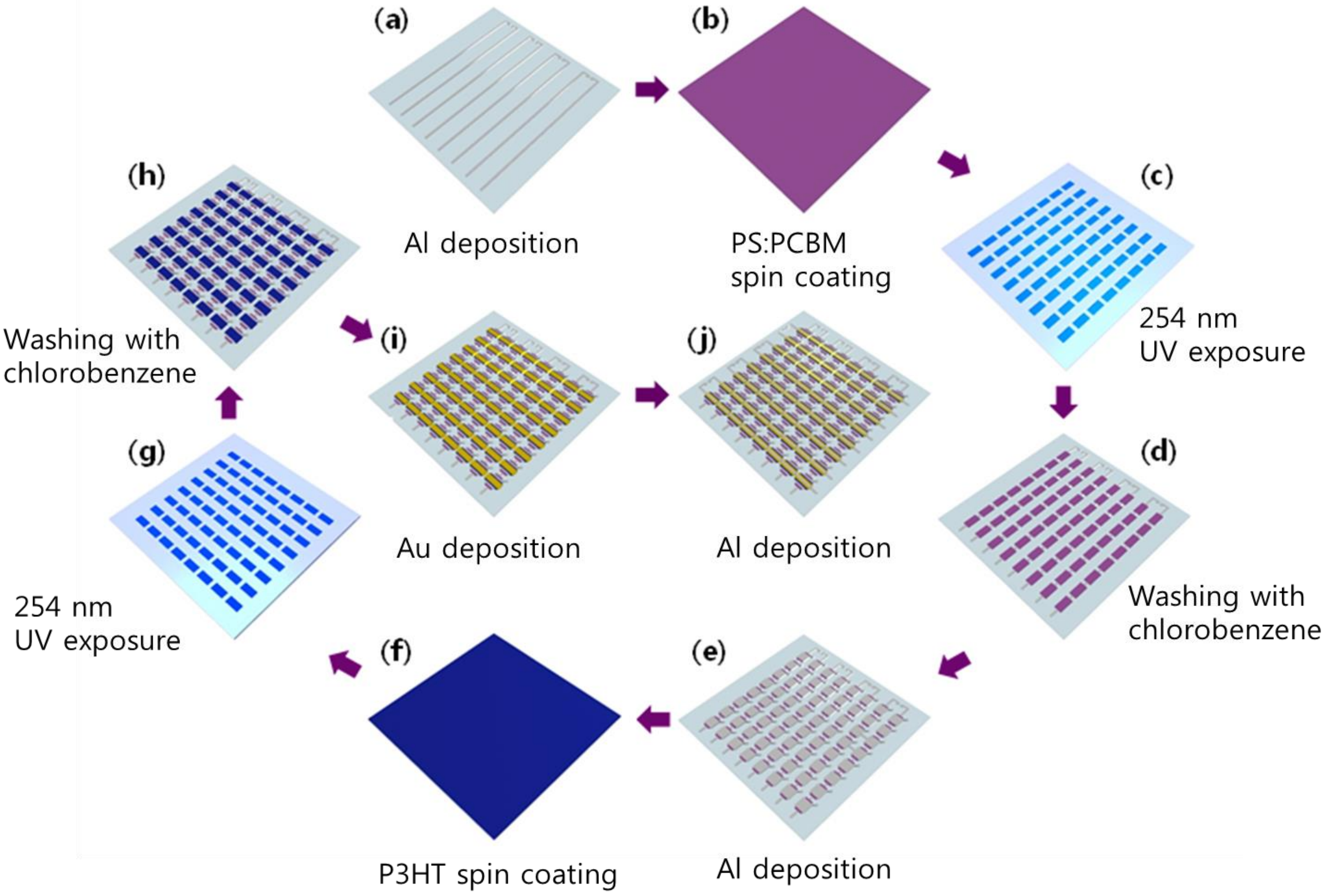
Poly(3-hexylthiophene) (P3HT)

- UV source

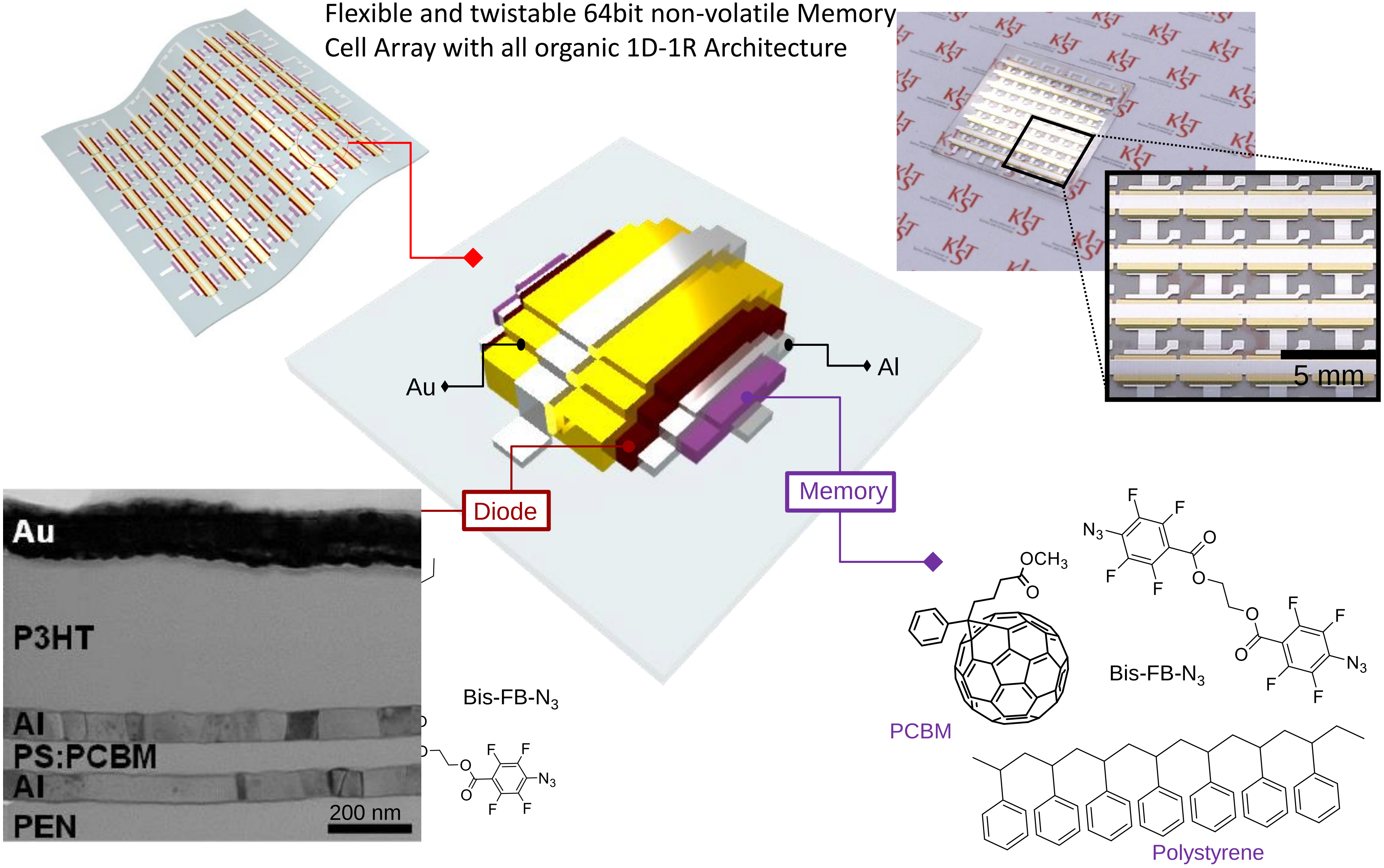
Wavelength: 254nm, 4W

1D-1R Architecture for Organic Non-volatile Memory

- Fabrication procedure of All organic flexible one resistor-one diode cell array



1D-1R Architecture for Organic Non-volatile Memory

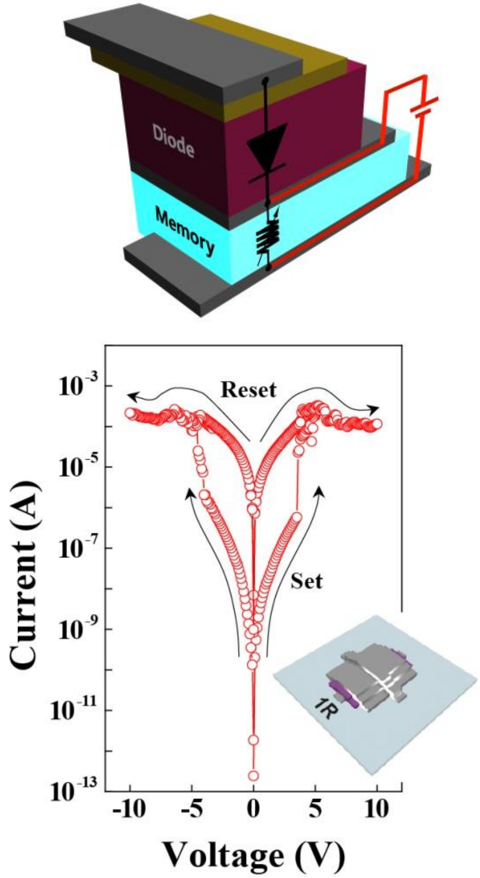


Flexible and twistable 64bit non-volatile Memory Cell Array with all organic 1D-1R Architecture

1D-1R Architecture for Organic Non-volatile Memory

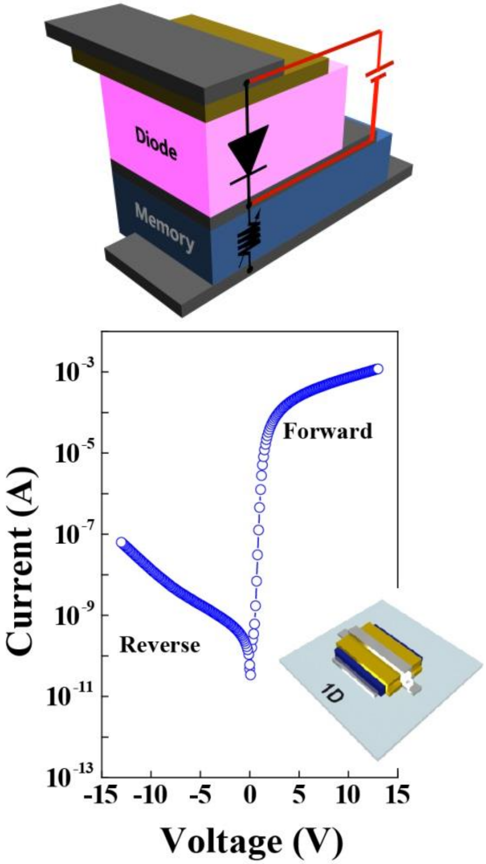
- I-V characteristics of 1D-1R Organic Non-volatile Memory Cell

Memory



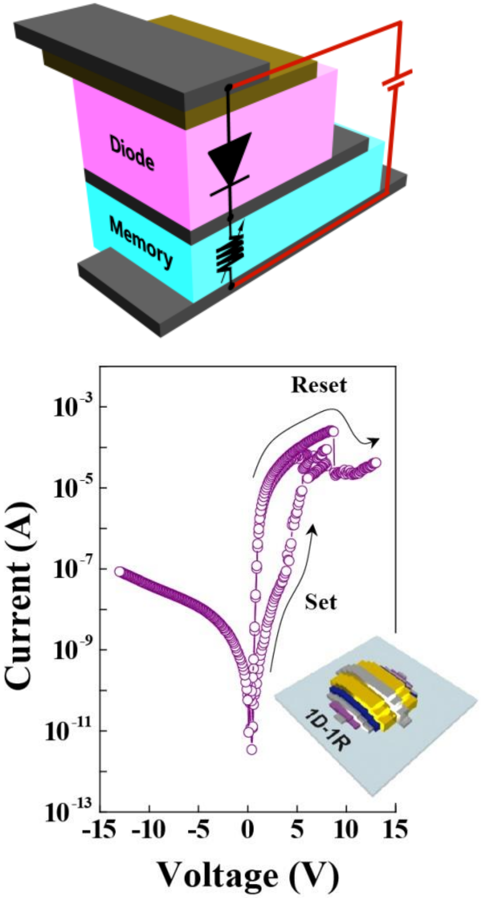
+

Diode



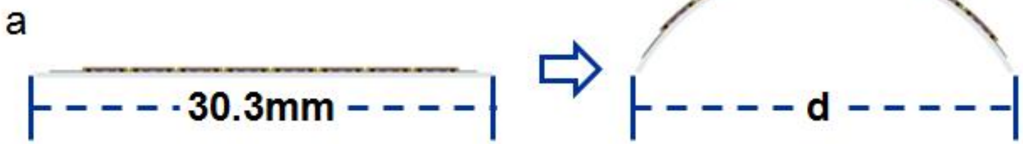
=

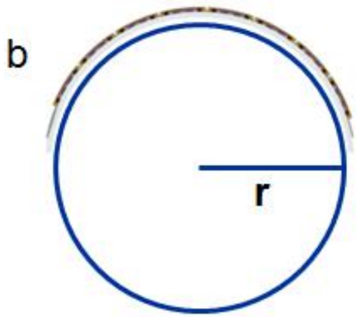
1D-1R



1D-1R Architecture for Organic Non-volatile Memory

Bending method

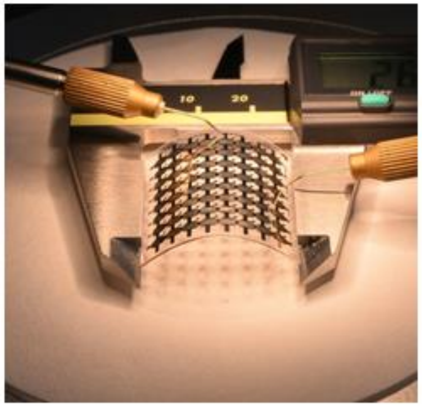




c

Distance (mm)	Radius (mm)	Strain (%)
30.30	∞	0.00
29.70	34.00	0.18
29.10	22.03	0.29
28.50	20.00	0.31
27.90	15.80	0.40
27.30	15.50	0.41
26.70	14.10	0.45
26.10	13.00	0.48
22.10	9.60	0.65
18.10	7.60	0.83
14.10	6.20	1.01
10.10	5.00	1.26
6.80 (Glass pipet)	3.40	1.85
6.30 (Breakdown of diode)	3.10	2.03
5.00 (5 sheets of glass)	2.50	2.51
4.00 (4 sheets of glass)	2.00	3.14
3.00 (3 sheets of glass)	1.50	4.19
2.00 (2 sheets of glass)	1.00	6.28
1.00 (1 sheet of glass) (Device is broken)	0.50	12.57

d



e

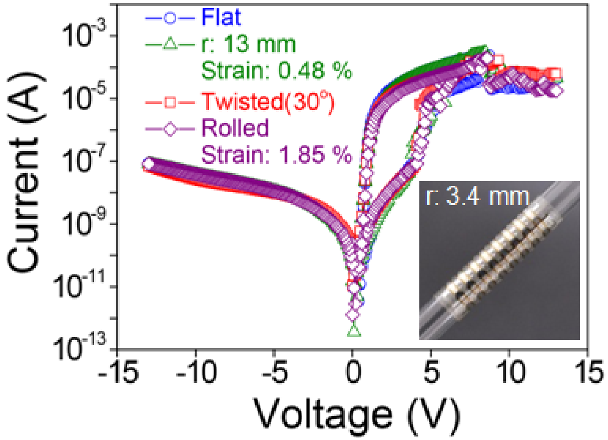
Thickness of glass:
1.00 mm

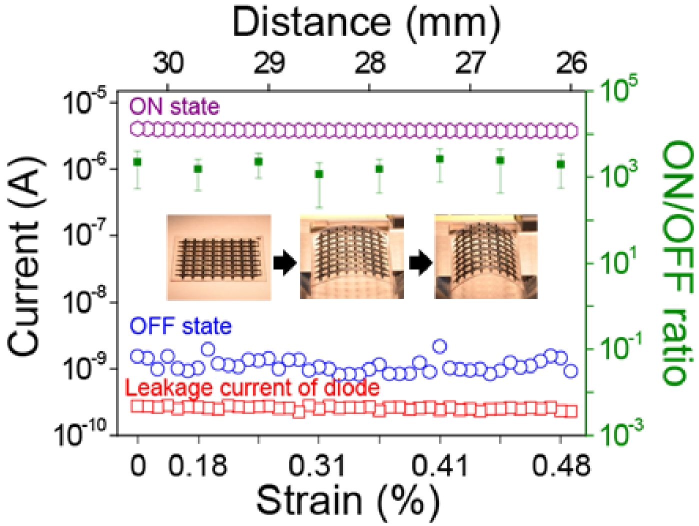
Equation of strain

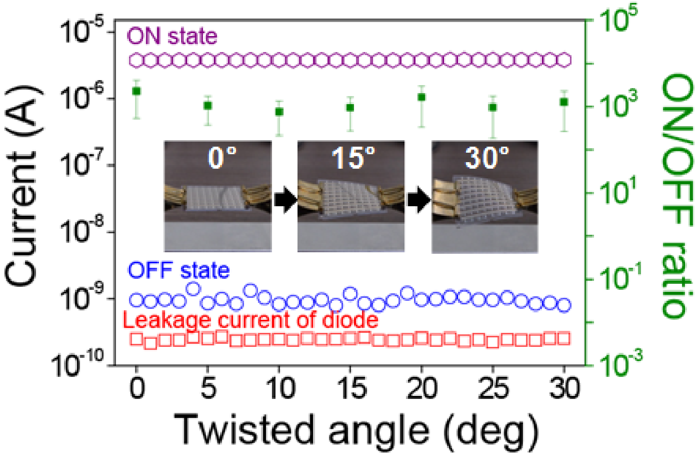
$$Strain\ (\%) = \frac{Total\ thickness\ of\ device}{2 \times radius\ of\ curvature} \times 100$$

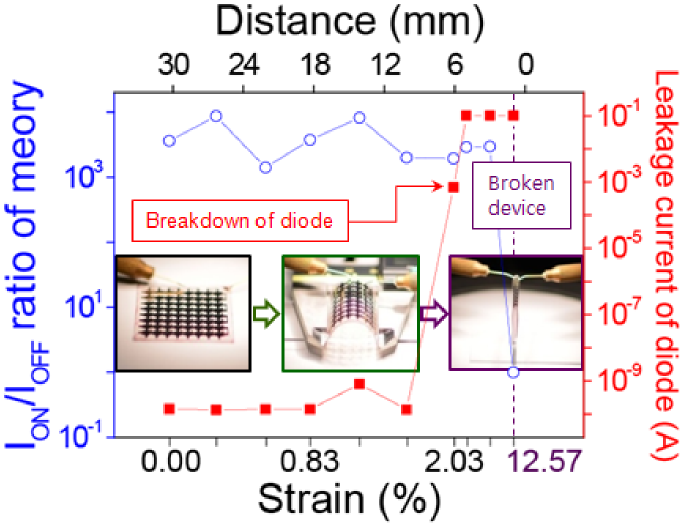
1D-1R Architecture for Organic Non-volatile Memory

- Memory Performances of 1D-1R Under various bending conditions



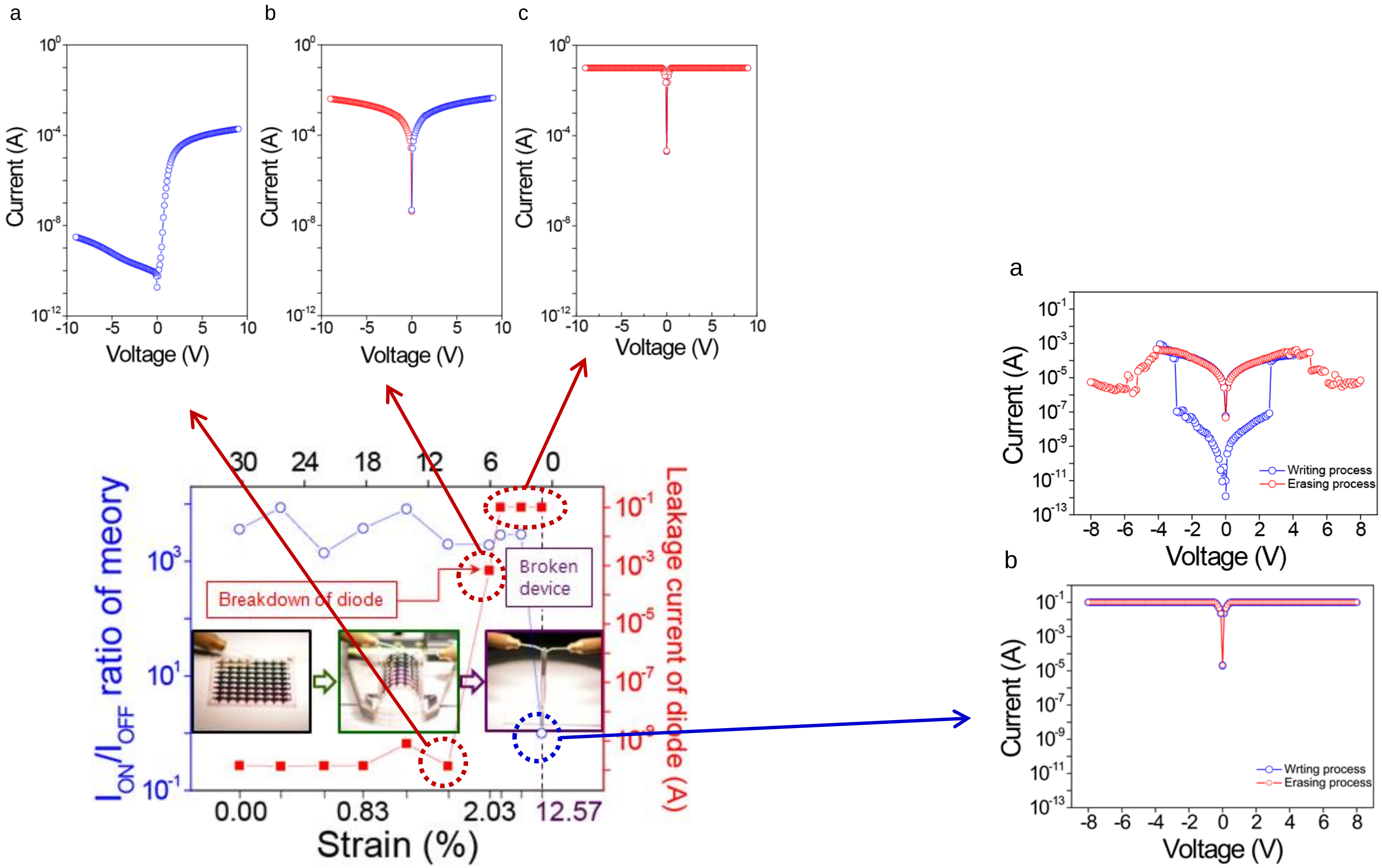






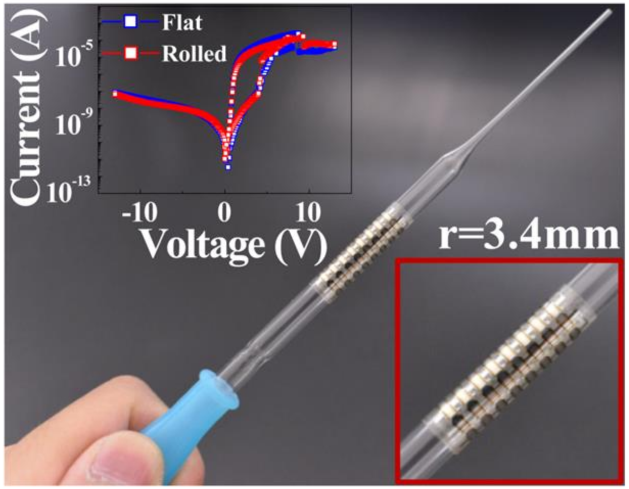
1D-1R Architecture for Organic Non-volatile Memory

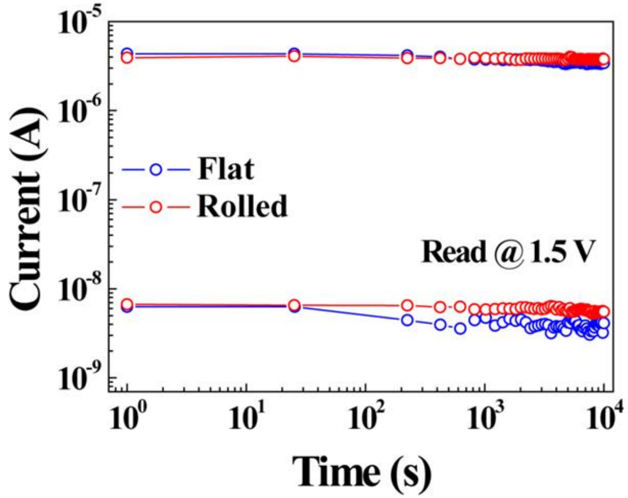
- Memory Performances of 1D-1R Under various bending conditions

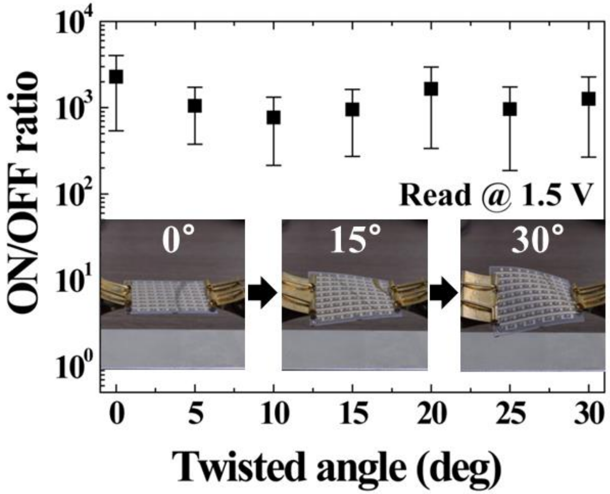


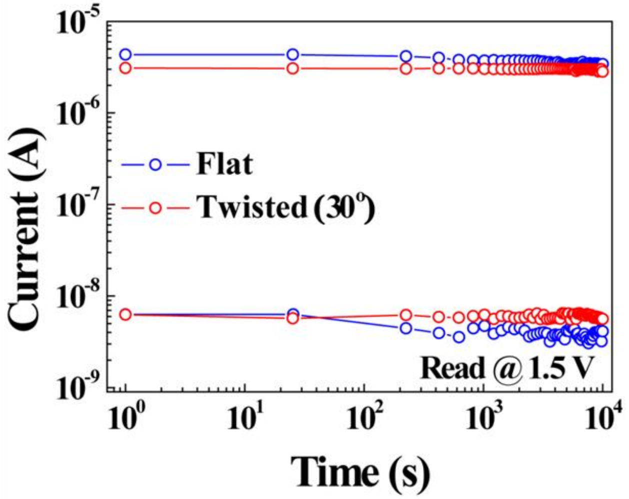
1D-1R Architecture for Organic Non-volatile Memory

- Memory Performances of 1D-1R Under various bending conditions



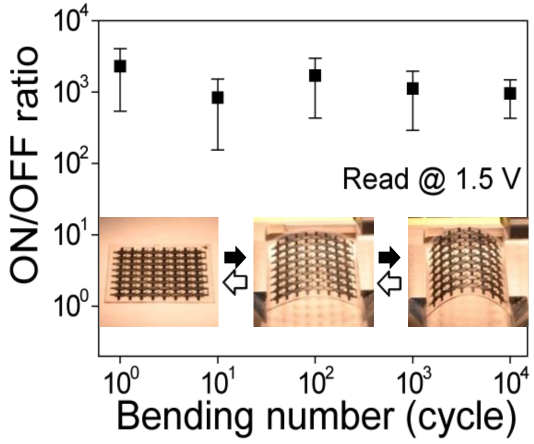


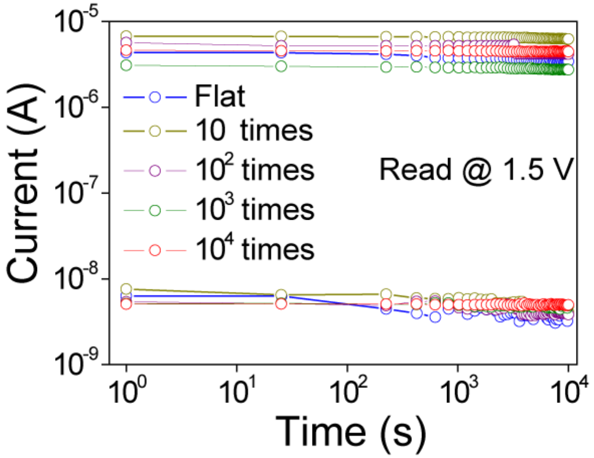


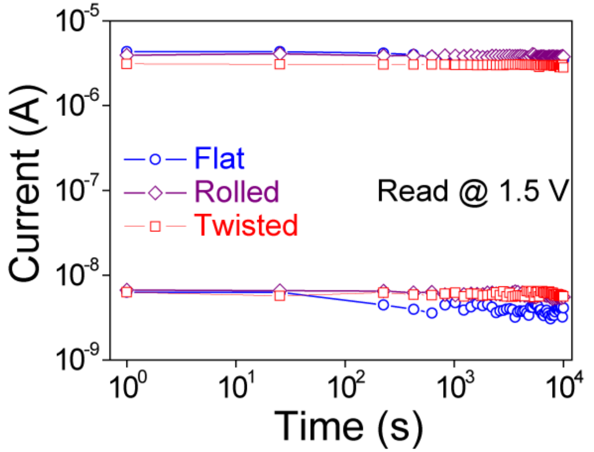


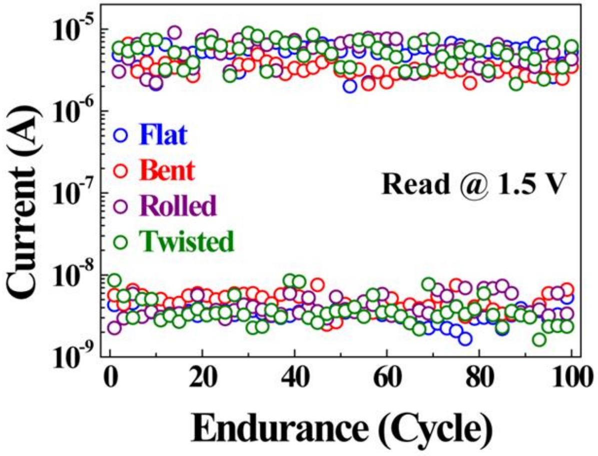
1D-1R Architecture for Organic Non-volatile Memory

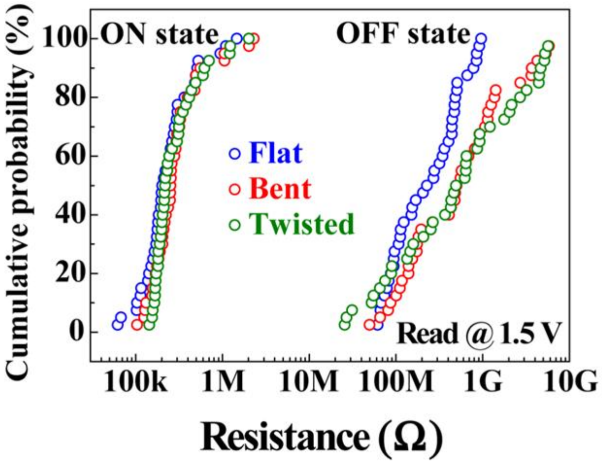
- Reliability of 1D-1R Under various bending conditions

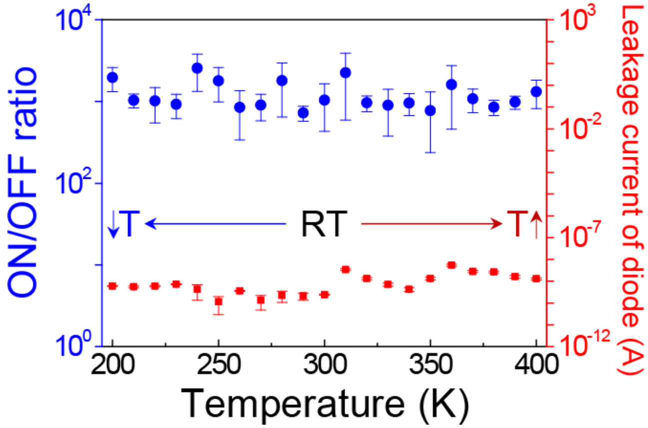






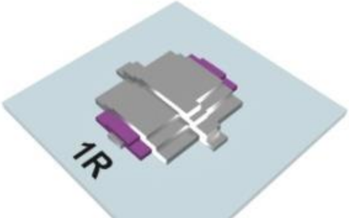


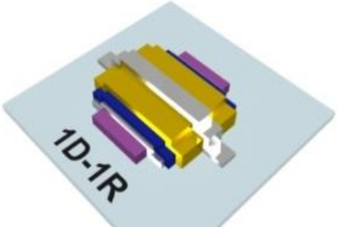


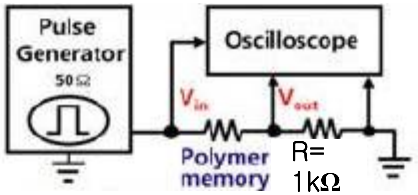


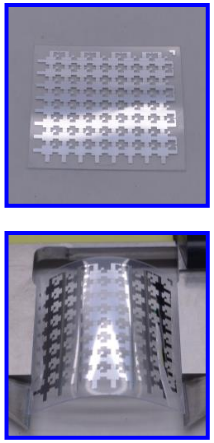
1D-1R Architecture for Organic Non-volatile Memory

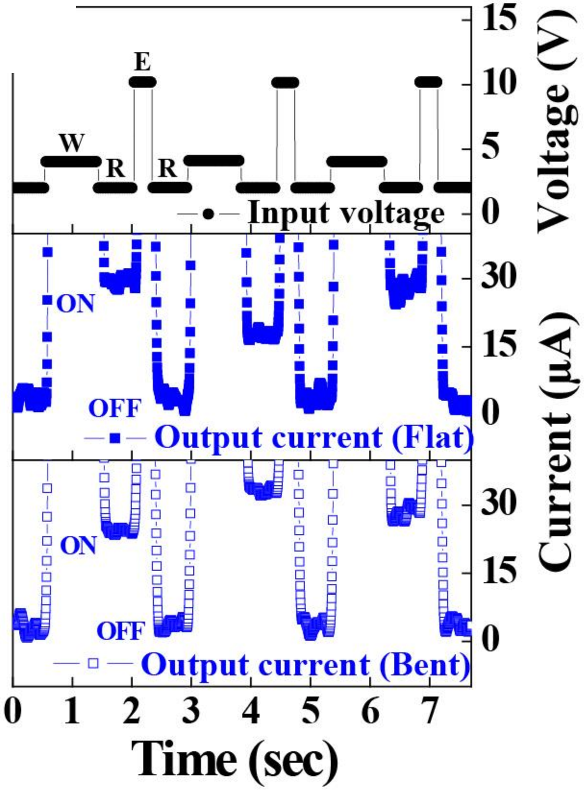
- Pulse Response test of bent 1D-1R cell

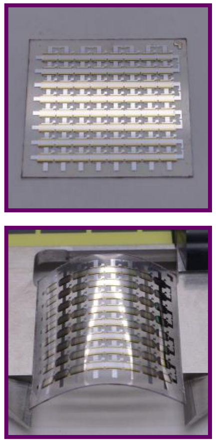


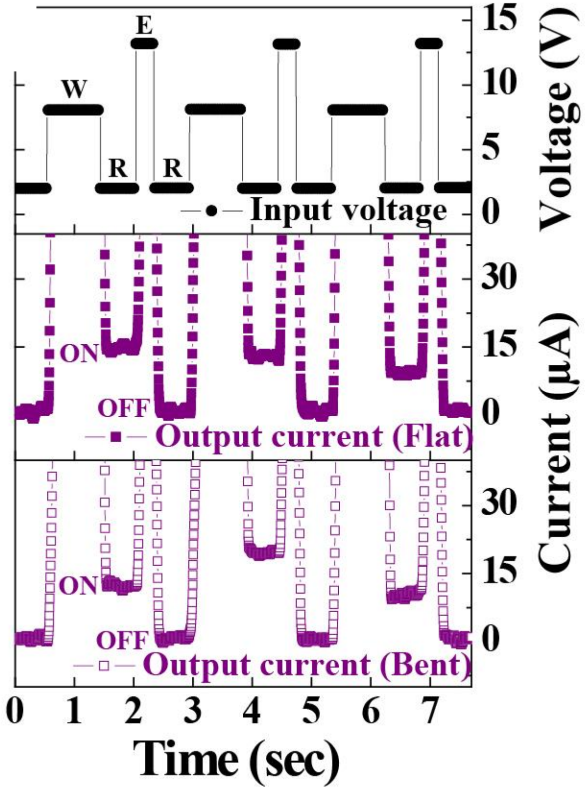






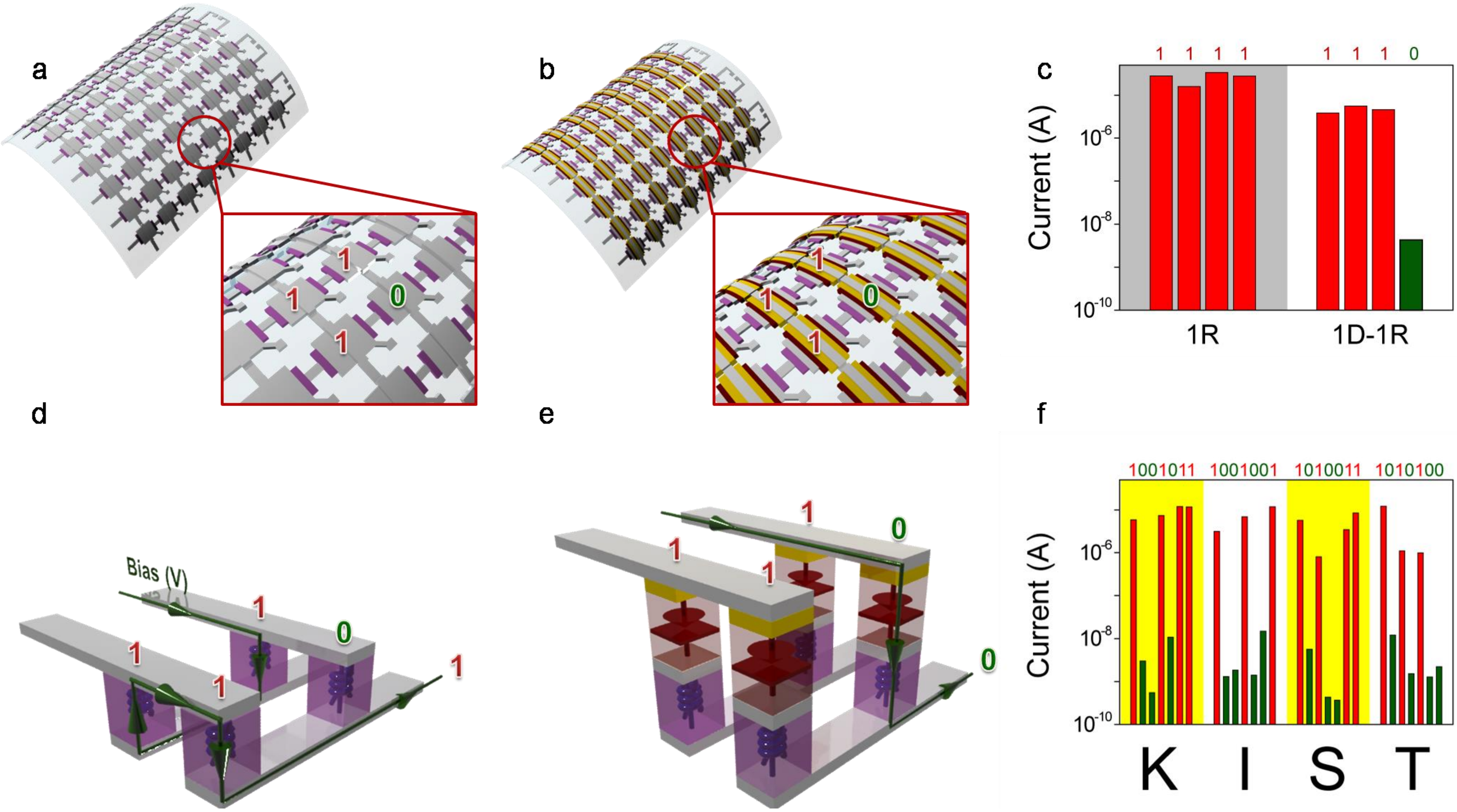






1D-1R Architecture for Organic Non-volatile Memory

- Addressing Test of Flexible 1R cell array vs. 1D-1R cell array



1D-1R Architecture for Organic Non-volatile Memory

nature COMMUNICATIONS

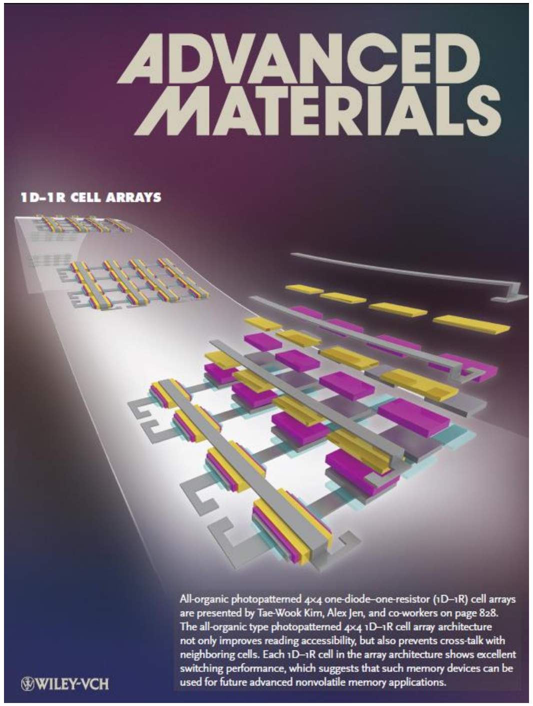
ARTICLE

Received 19 Jul 2013 | Accepted 3 Oct 2013 | Published 1 Nov 2013

DOI: 10.1038/ncomms3707

Flexible and twistable non-volatile memory cell array with all-organic one diode–one resistor architecture

Yongsung Ji[1,2], David F. Zeigler[3], Dong Su Lee[1], Hyejung Choi[4], Alex K.-Y. Jen[3], Heung Cho Ko[2] & Tae-Wook Kim[1]



All-organic photopatterned 4×4 one-diode–one-resistor (1D–1R) cell arrays are presented by Tae-Wook Kim, Alex Jen, and co-workers on page 828. The all-organic type photopatterned 4×4 1D–1R cell array architecture not only improves reading accessibility, but also prevents cross-talk with neighboring cells. Each 1D–1R cell in the array architecture shows excellent switching performance, which suggests that such memory devices can be used for future advanced nonvolatile memory applications.

Kim *et al*, Advanced Materials, 24, 828 (2012) Frontispiece of advanced materials

Ji *et a*l, Nature Communications 4:2707 | DOI: 10.1038/ncomms3707 (2013)

Organic Non-volatile Memory Transistors

Organic Non-volatile Memory Transistors

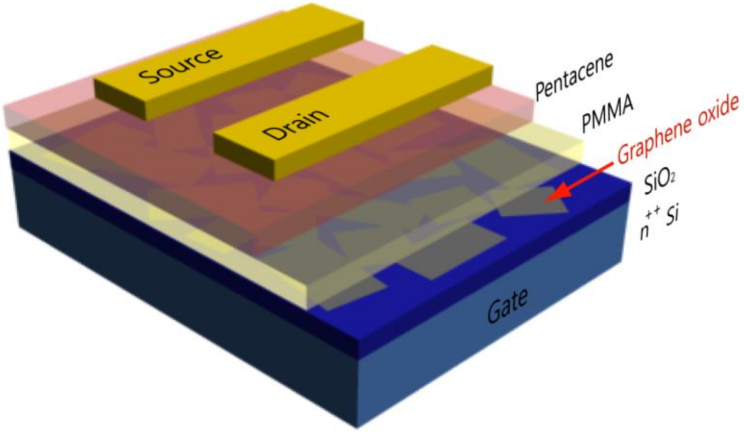
Low voltage memory transistor with hybrid gate dielectrics

Organic transistors with small molecule charge trap layers

One step synthesis of Au nanoparticle-cyclized polyacrylonitrile composite films

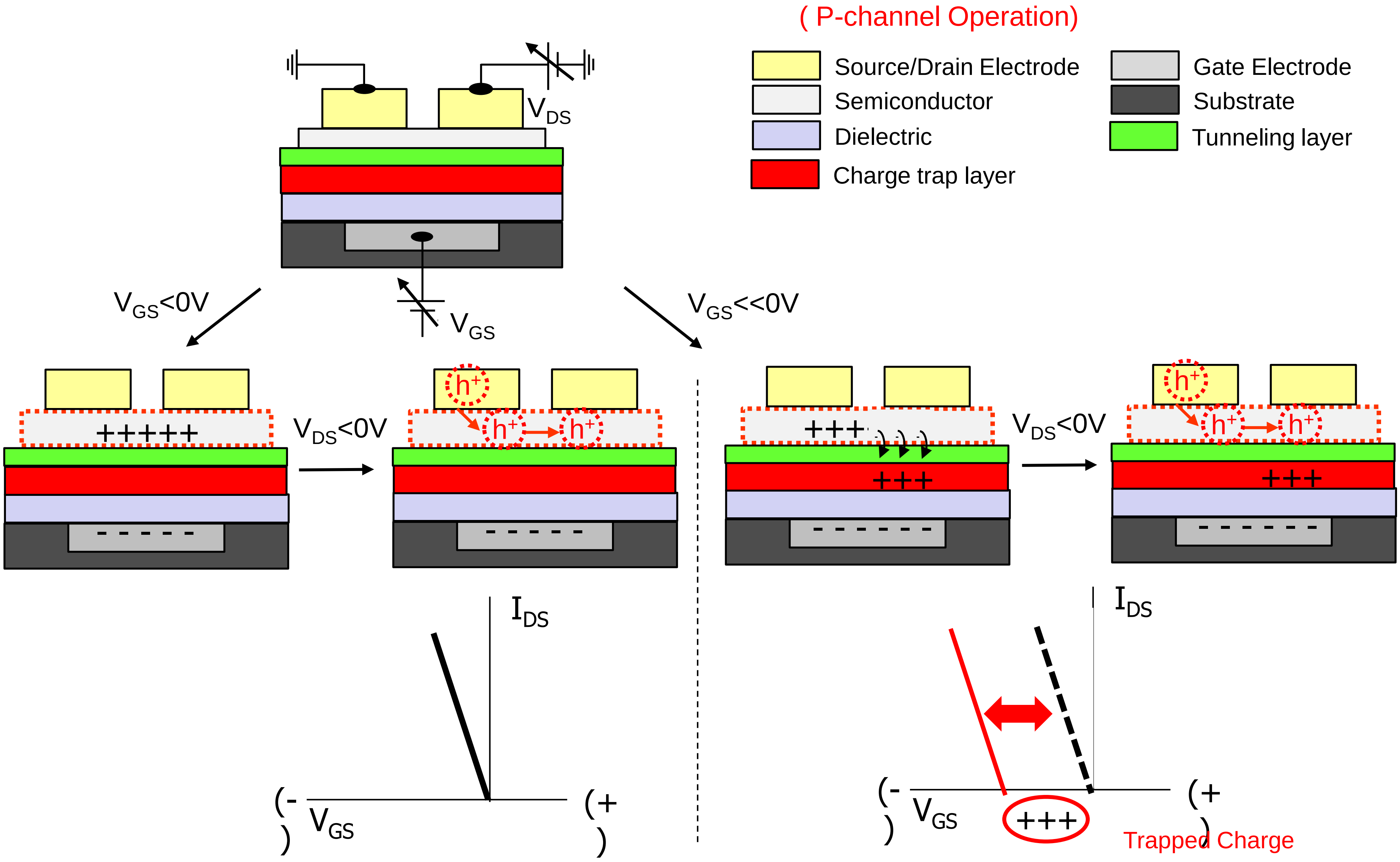
Graphene quantum dots for organic non-volatile memory transistors

Control of ferroelectricity of P(VDF-TrFE) copolymer via photocrosslinking



Kim *et al*, Applied Physics Letters 97, 023310 (2010)
Kim *et al*, Organic Electronics 15, 2775 (2014)
Cho *et al*, Journal of Materials Chemistry C, 4, 1511 (2016)
Ji *et al*, Nanotechnology, 27, 145204 (2016)
Jang *et al*, Manuscript in preparation (2017)

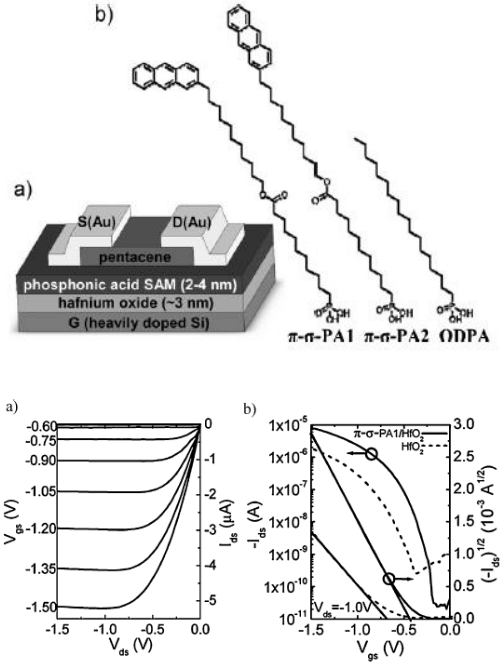
Operation of Organic Memory Transistors



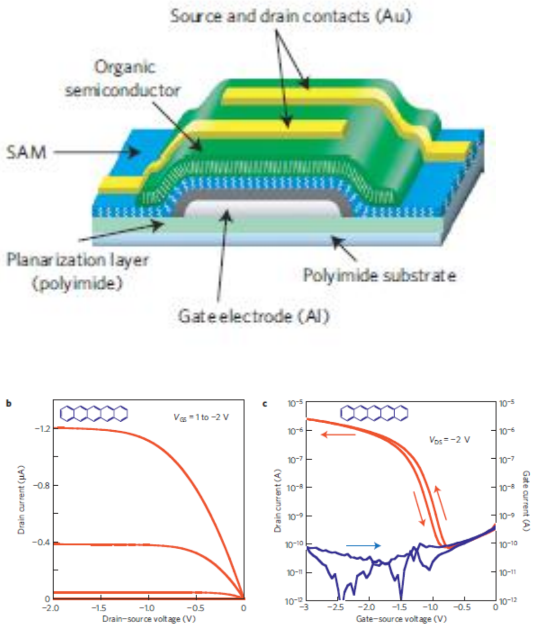
Previous Research on Organic Memory Transistors

- Researches low voltage organic field effect transistors

Hybrid gate dielectric

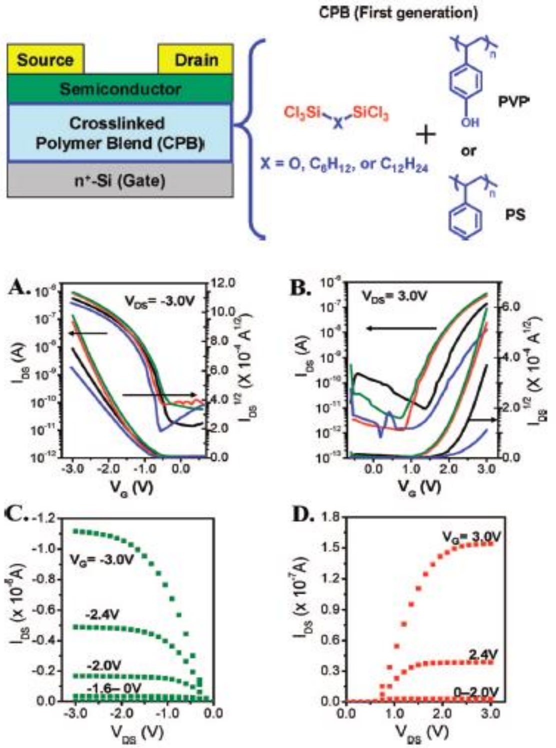


O. Acton et al, **Adv. Mater.,** 20, 3697 (2008)



T. Sekitani et al, **Nature Mat.,** Vol 9, 1015 (2010)

Ultrathin organic gate dielectrics



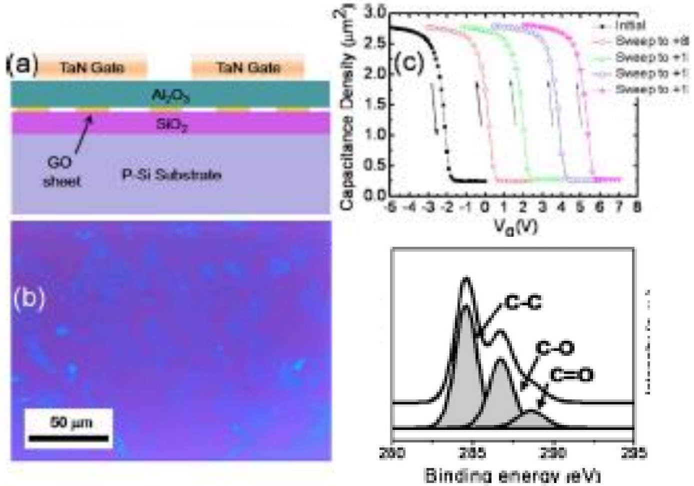
C. Kim et al, **JACS,** 130, 6867 (2008)

Hybrid gate dielectrics such as sol-gel HfOx+SAMs or AlOx+SAMs and Ultrathin organic gate dielectrics are widely used for low voltage organic field effect transistors.

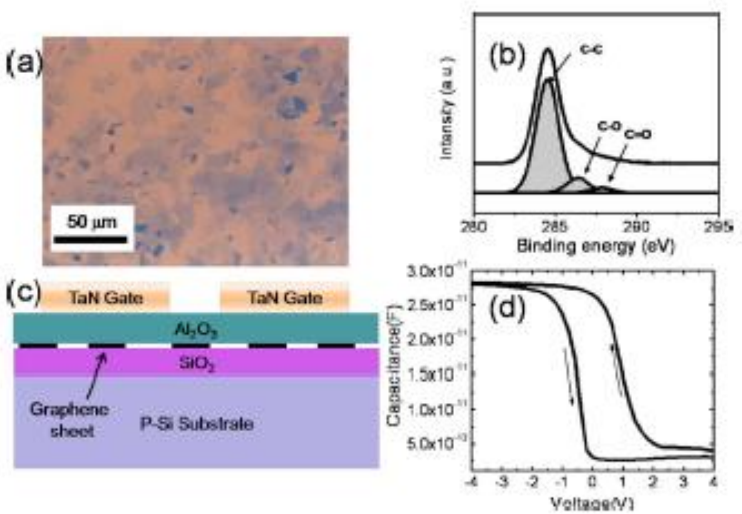
→ If we use graphene oxide layer as a charge trap layer in this low voltage OFET platform, we are able to demonstrate low voltage organic memory transistors.

Previous Research on Organic Memory Transistors

- Why graphene oxide for organic memory transistors?



Post annealing process



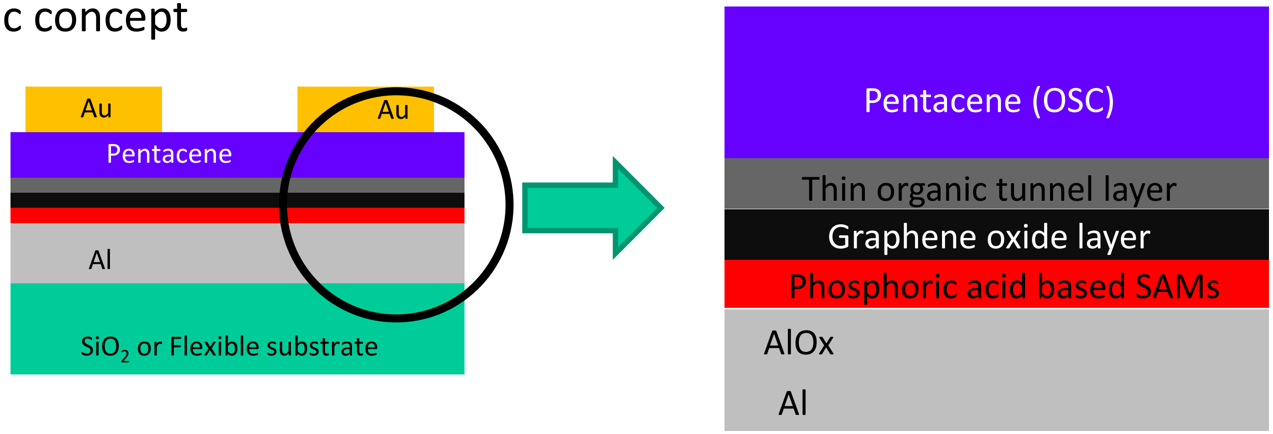
In flash type memory device, post annealing is necessary tor achieving dense blocking oxide(Al_2O_3, in this case). However this post annealing process reduce graphene oxide to graphene and that has poor charge trap behavior than that of graphene oxide(narrowing CV hysteresis after post annealing process)

Organic memory transistors do not need such a high post annealing, hence GO is more useful charge trap layer in organic memory transistors.
One more advantage of GO is that it is solution-processable (spin-coating) and ink-jet printable, so it is compatible with memory storage system based on flexible organic electronics.

GO based Low Voltage Organic Memory Transistors

- Graphene oxide + Hybrid gate dielectric(AlO$_x$+SAMs)

Basic concept



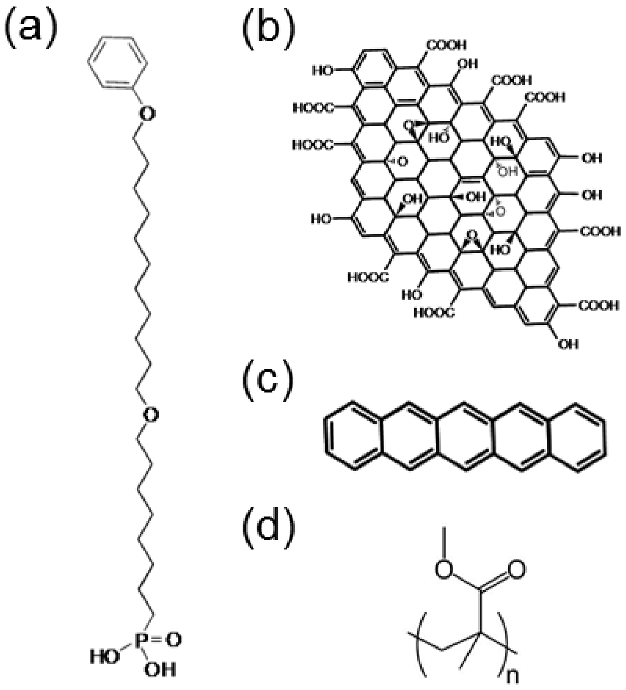
In our previous research, We clearly showed that grahpene oxide is one of the charge trap layers for high performance organic memory transistors.

Fabrication process issue

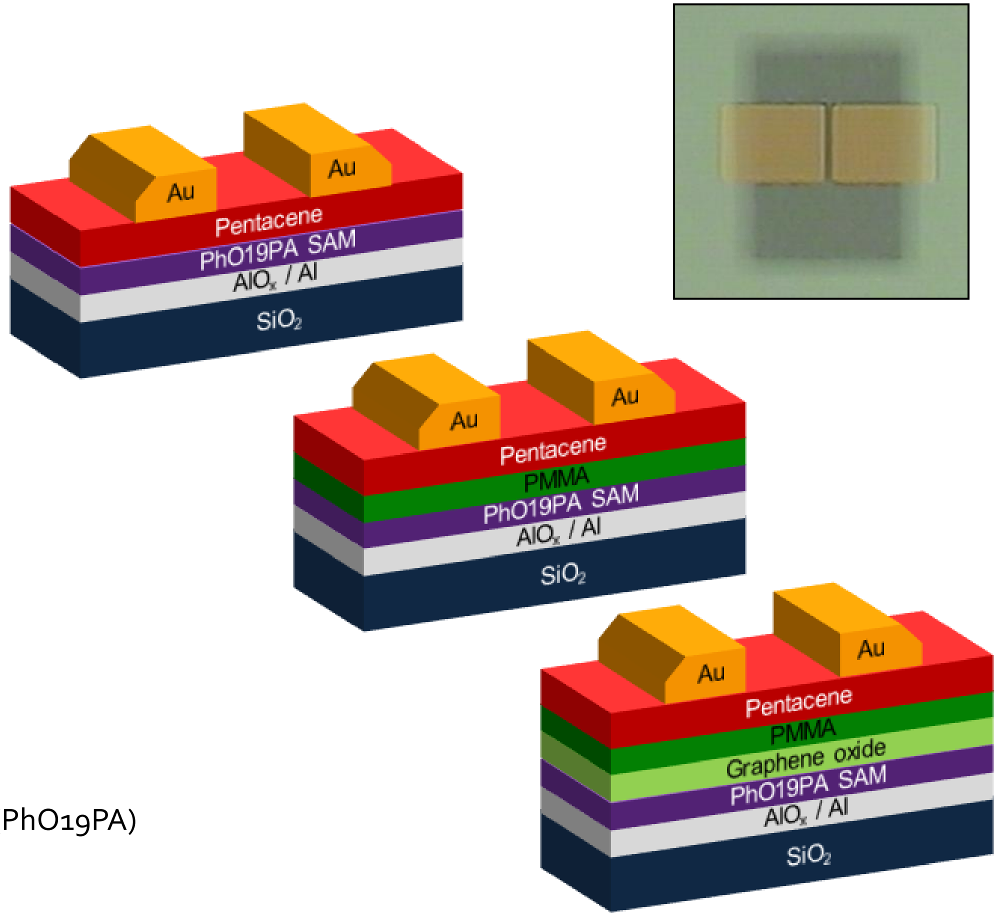
- Control of breakdown voltage of hybrid gate dielectrics
- Formation of SAMs on AlOx
- Spin coating of graphene oxide on SAMs layer uniformly
- Materials selection and thickness control of organic tunnel layer

GO based Low Voltage Organic Memory Transistors

- Graphene oxide + Hybrid gate dielectric(AlO_x+SAMs)



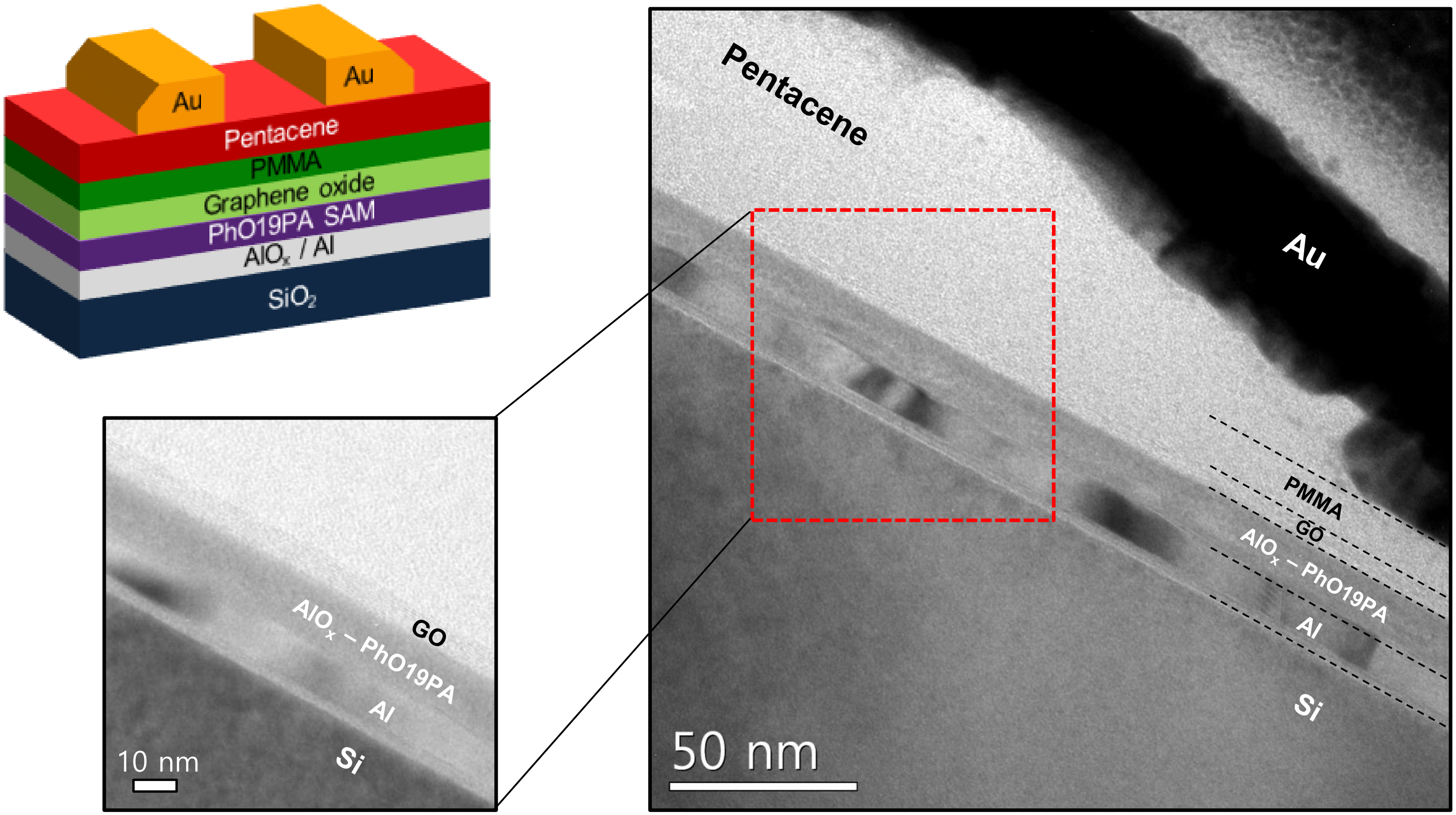
(a) [8-(11-phenoxy-undecyloxy)-octyl]phosphonic acid (PhO19PA)
(b) Graphene oxide
(c) Pentacene
(d) PMMA



Kim *et al*, Organic Electronics 15, 2775 (2014)

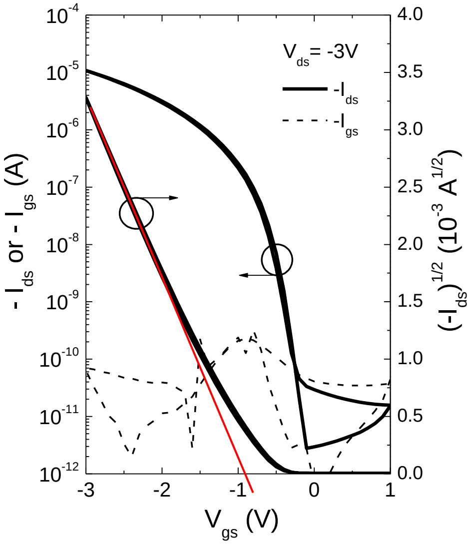
GO based Low Voltage Organic Memory Transistors

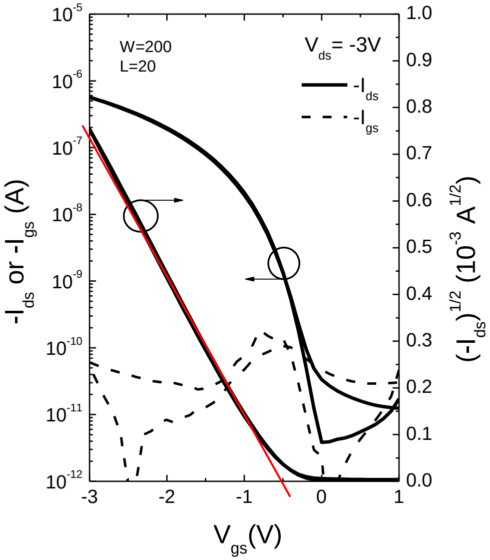
- Cross-sectional TEM image

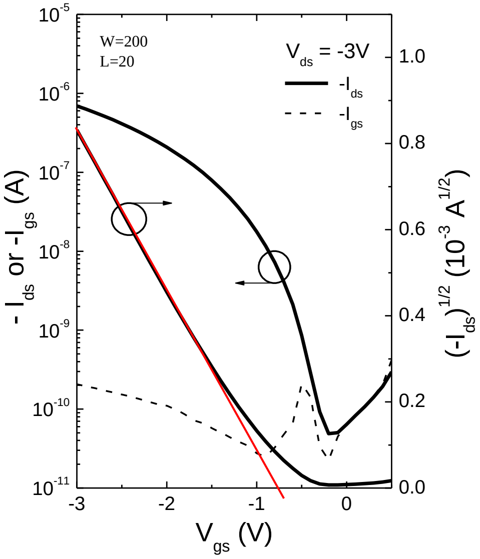


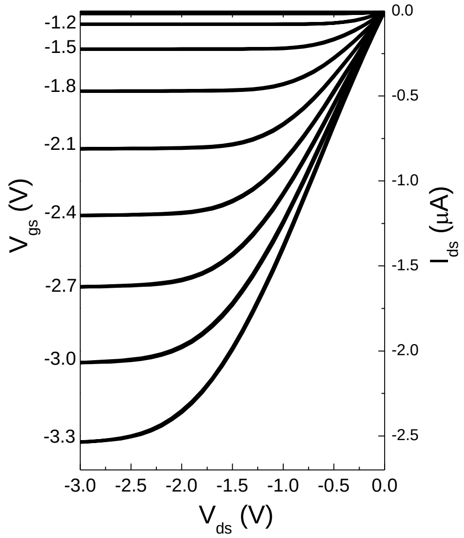
GO based Low Voltage Organic Memory Transistors

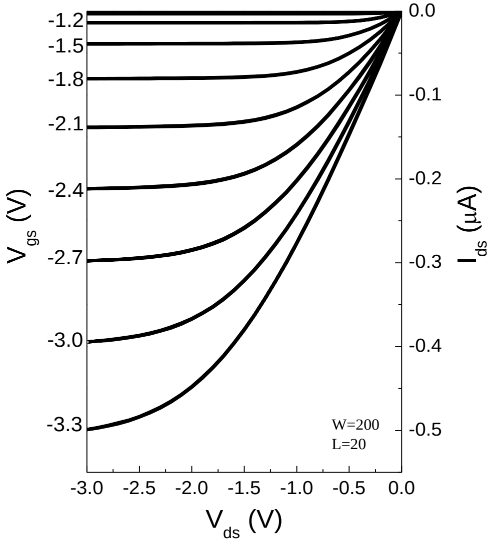
- Transfer and output characteristics





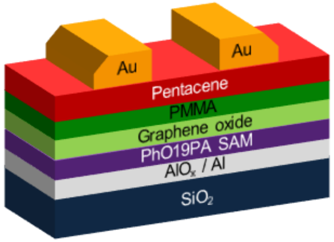


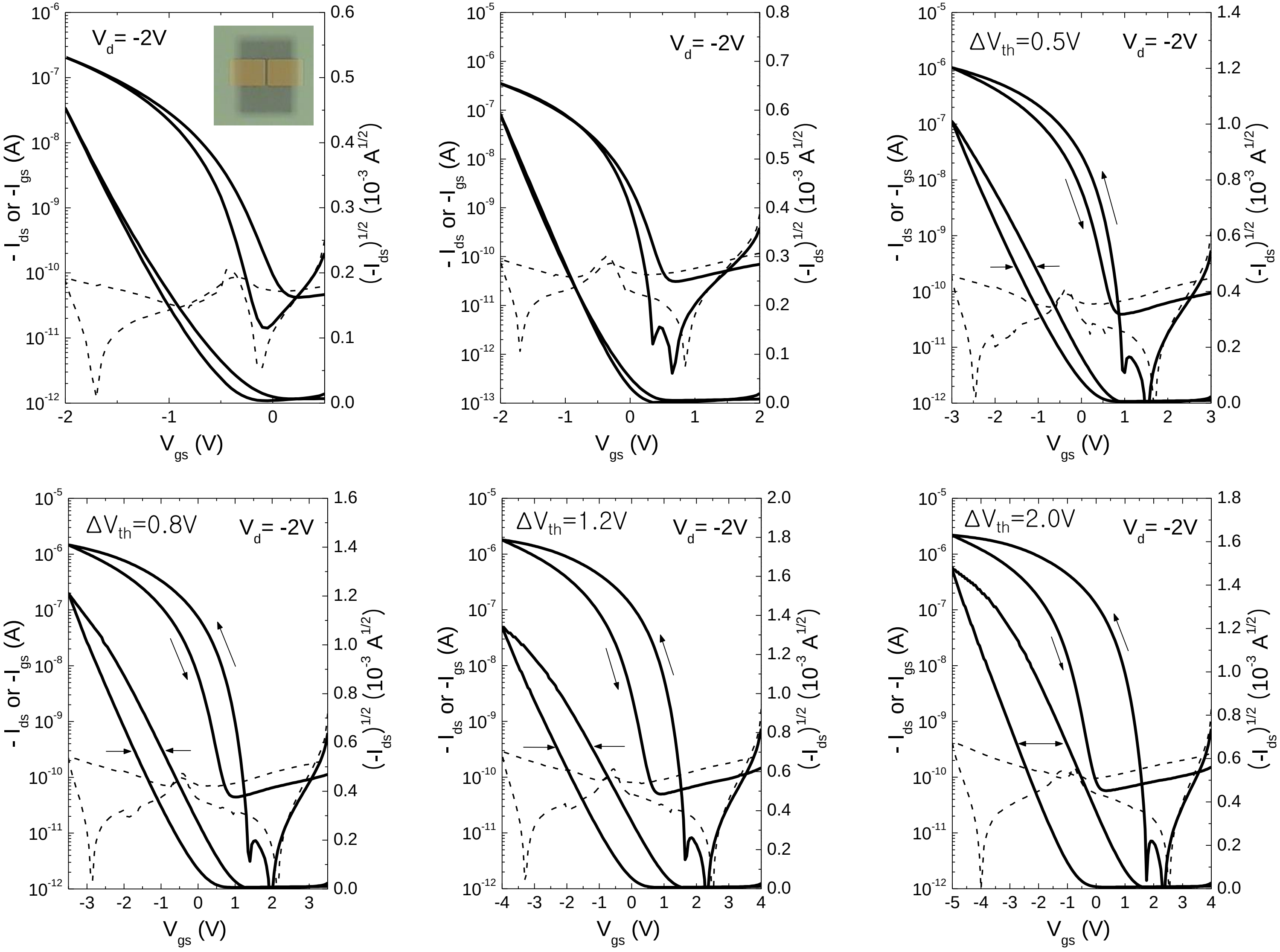




GO based Low Voltage Organic Memory Transistors

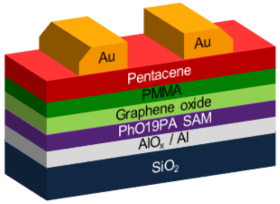
- Sweep Hysteresis

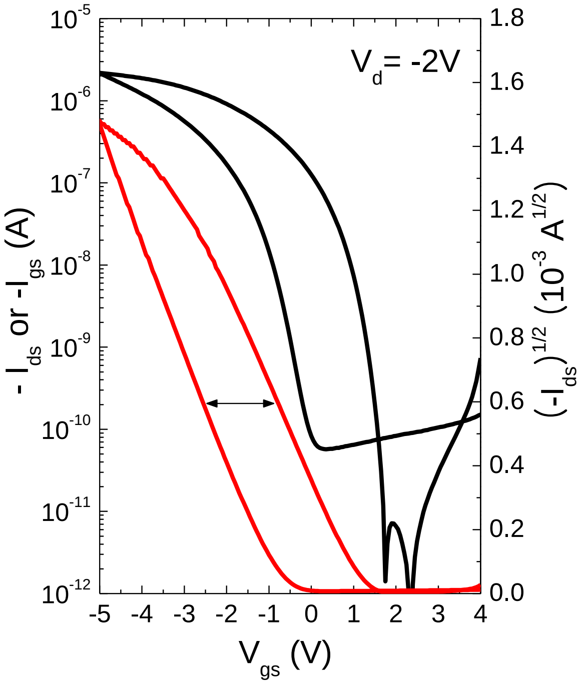




GO based Low Voltage Organic Memory Transistors

- Calculation of stored charges on Graphene oxide





The amount of the trapped charges at the graphene oxide layer was calculated

$$\Delta V_{th} = - d_i Q/\varepsilon_i = - Q/C_i$$

ΔV_{th} : the hysteresis window of memory transistor
Q : the traped charge
C_i : the total capacitance of the gate dielectrics

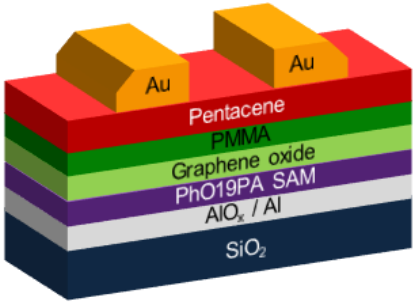
Total amount of charge on thick graphene oxide (9nm)
~ 2.9×10^{12} cm^{-2}

From ΔV_{th} = 2.0V and C_i = 233 nF/cm^2.

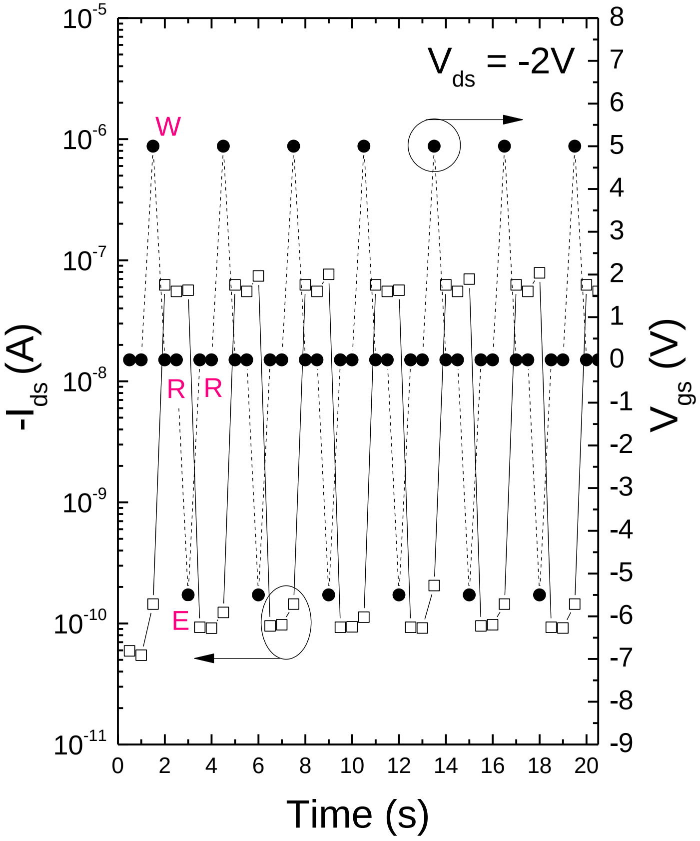
Monolayer of graphene oxide sheet has trap density of 3.22×10^{11} cm^{-2}

GO based Low Voltage Organic Memory Transistors

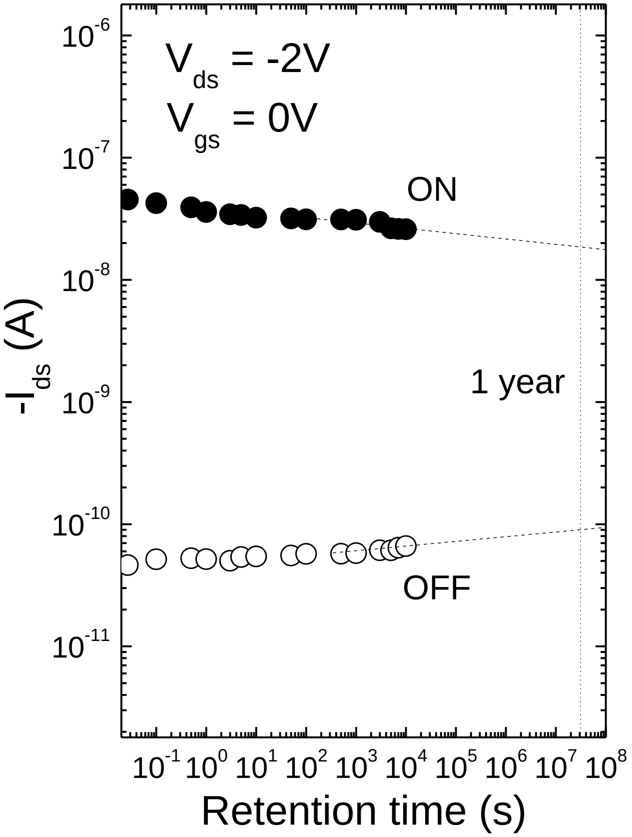
- Device performances



WRER Test

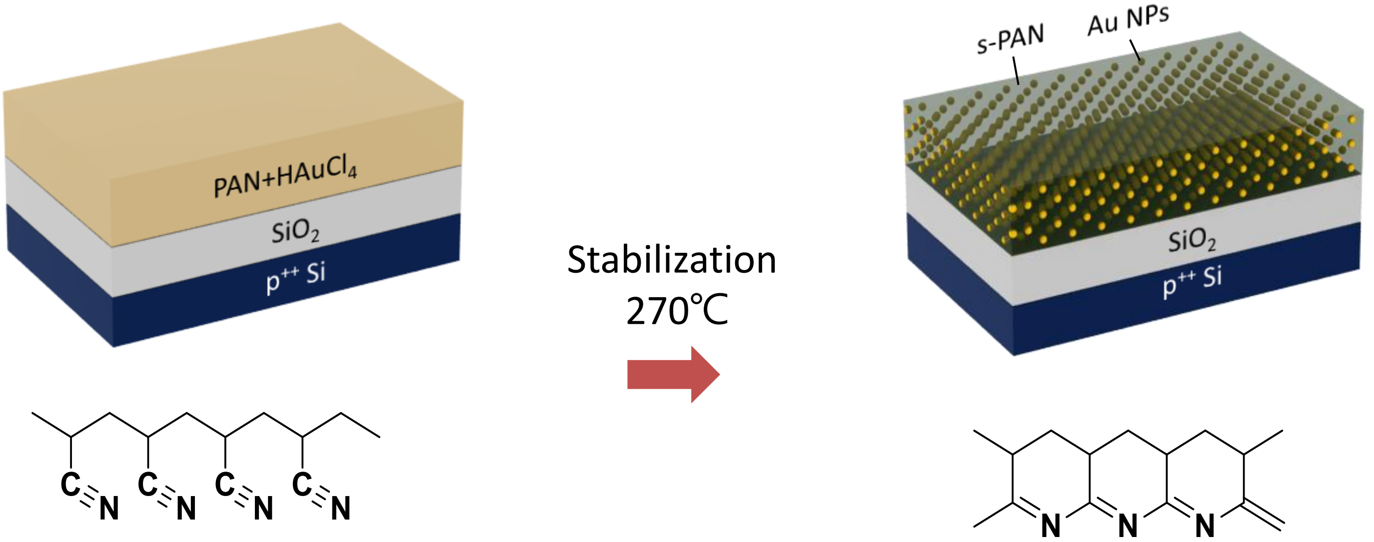


Data Retention



Organic Memory Transistors with One step synthesized Au NPs

- One step synthesis of Au nanoparticle-cyclized polyacrylonitrile composite films



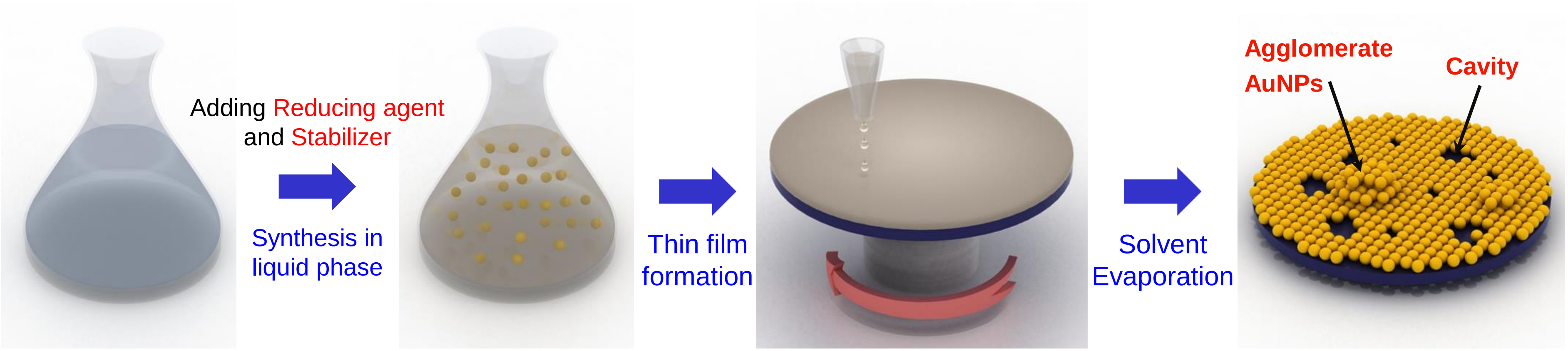
Stabilization
270℃

Polyacrylonitrile (PAN)

Cyclized PAN (cPAN)

Cho *et al*, *Journal of Materials Chemistry C*, 4, 1511 (2016)

Conventional processes of Au NPs in device application



Adding Reducing agent and Stabilizer

Synthesis in liquid phase

Thin film formation

Solvent Evaporation

Agglomerate AuNPs

Cavity

$HAuCl_4$
(Gold salt solution)

AuNPs in
liquid solution

Spin-coated
AuNPs solution

Non-uniform AuNPs
on the substrate

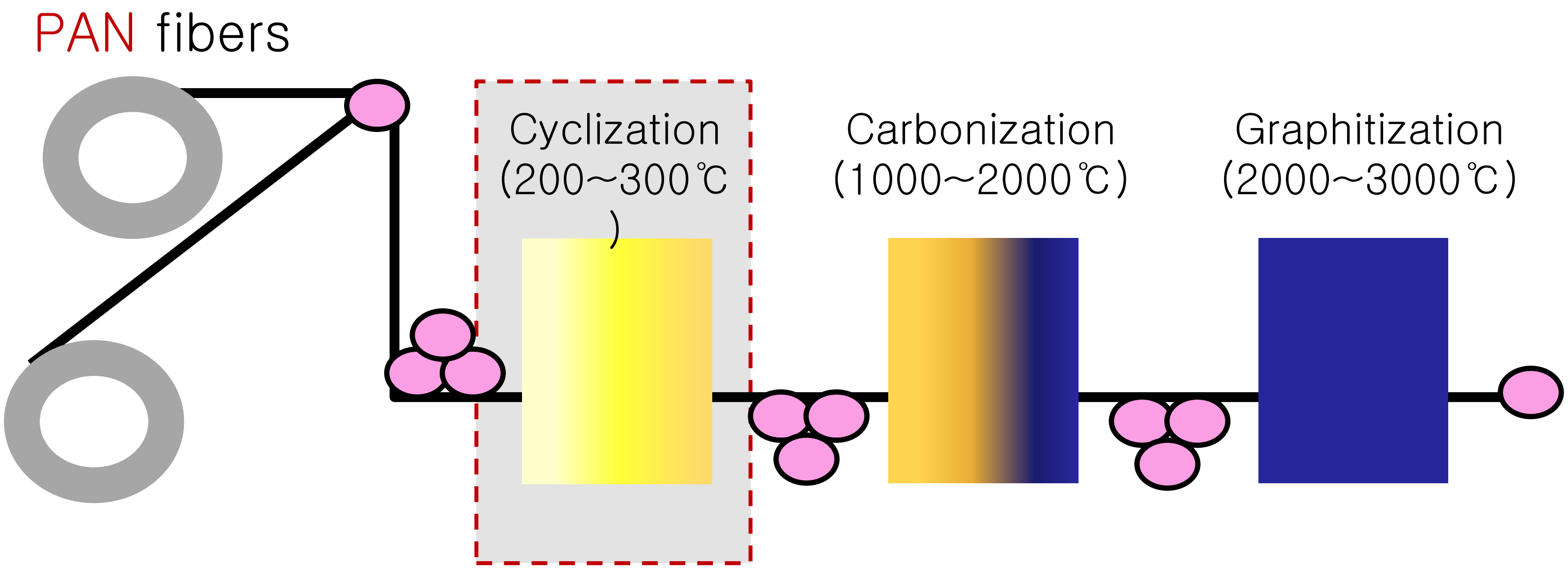
- AuNPs by a bottom-up method generally involves the chemical reduction of gold ions in a liquid phase with reducing agents and stabilizers.
- For actual device applications, additional thin film formation is essential after nanoparticle synthesis in liquid.

- Problem : This intricate process causes agglomeration, deformation of nanoparticles, and damage to an organic underlayer by interacting with the solvent or an additive, such as the reducing agent and the nanoparticle stabilizer, and causes a non-uniform dispersion in the matrix.

- For the NVM application, electrically isolated states of AuNPs are preferred.

Cyclization of Polyacrylonitile (PAN)

Conventional Carbon fiber process

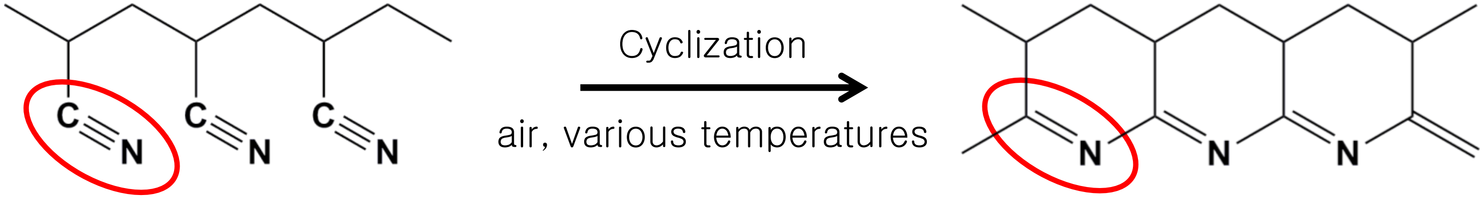


PAN fibers

Cyclization (200~300℃)

Carbonization (1000~2000℃)

Graphitization (2000~3000℃)



Cyclization

air, various temperatures

Polyacrylonitrile (PAN)

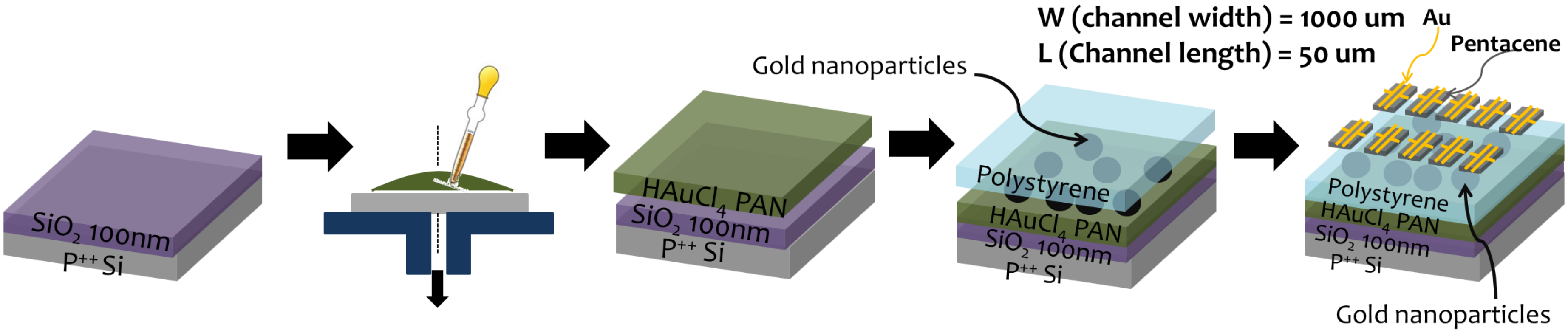
Cyclized PAN

converts from the nitrile group (–C≡N) into a ladder structure (–C=N)

Fiber ⇒ Film ?

Organic Memory Transistors with One step synthesized Au NPs

- Fabrication Process



Spin coated HAuCl$_4$ in PAN

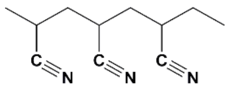
Cyclization at various temperatures for 2h in air

Tunneling layer Spin coating

Thermal evaporation in vacuum

- Materials & Conditions

Material (1) ◆ Solution preparation
*Polyacrylonitrile (PAN)
*Solvent : Dimethylformamide (DMF)
*The concentration of solution was 1.5 wt%

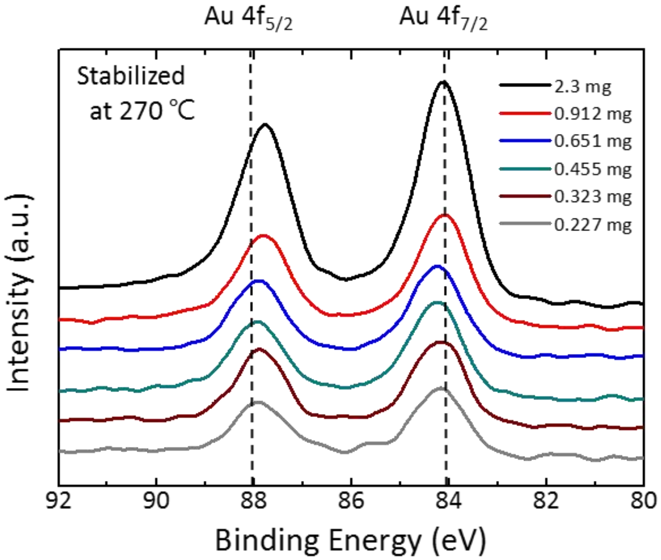


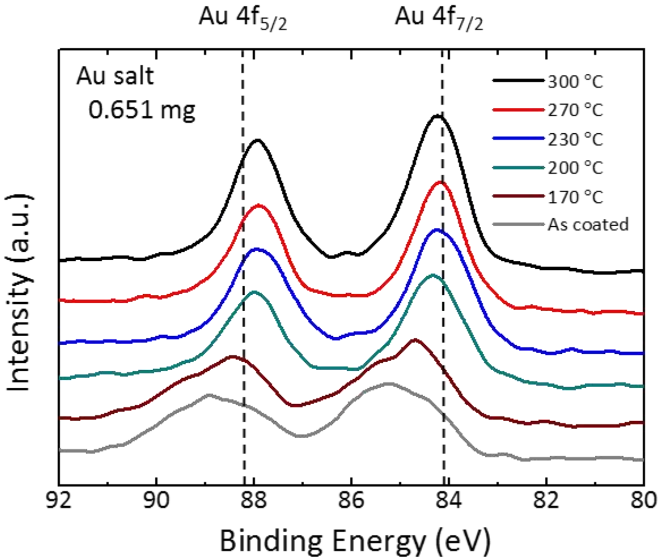
Material (2) ◆ Salt : HAuCl$_4$
*Solvent : PAN 1ml
*Spin-coating was performed under 500 rpm for 5 sec/4000 rpm for 90 sec

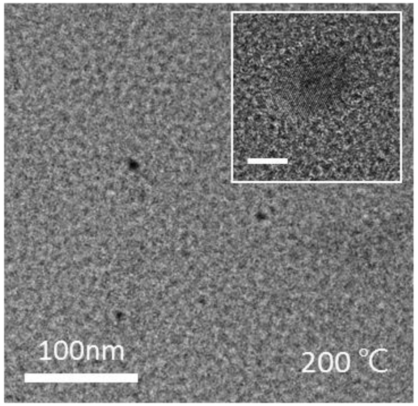
EXPERIMENTAL (1)		EXPERIMENTAL (2)	
Constant Ration	**Cyclization Temp.**	**Constant temperature**	**HAuCl$_4$ Ration (wt%)**
7:1 **(PAN : 1ml)**	**As spin coating**	**Cyclization at 270 ℃**	**2:1**
	170 ℃		**5:1**
	200 ℃		**7:1**
	230 ℃		**10:1**
	270 ℃		**15:1**
	300 ℃		**20:1**

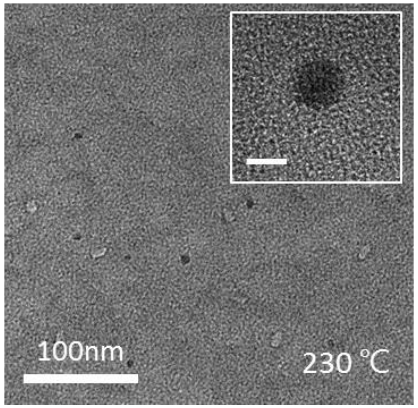
Organic Memory Transistors with One step synthesized Au NPs

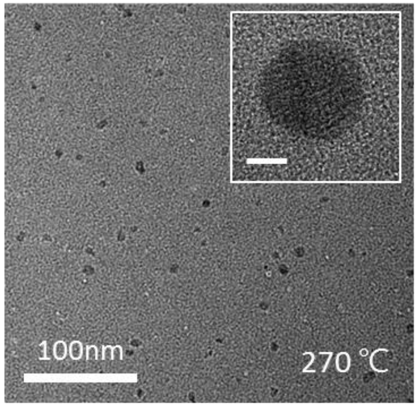
- XPS & TEM analysis





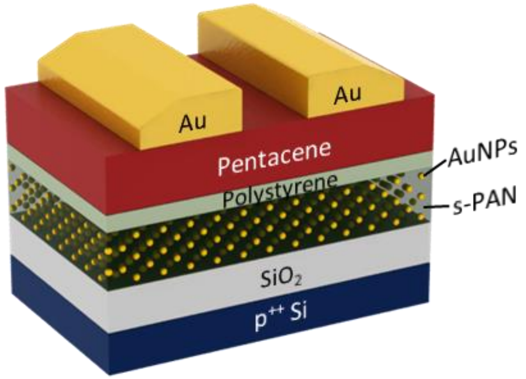


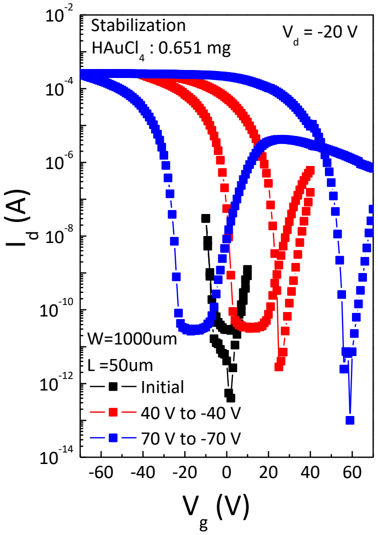


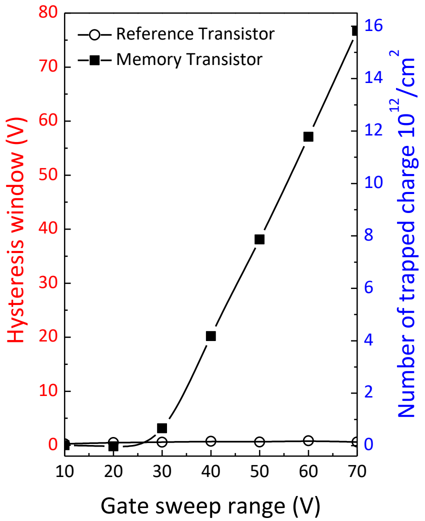


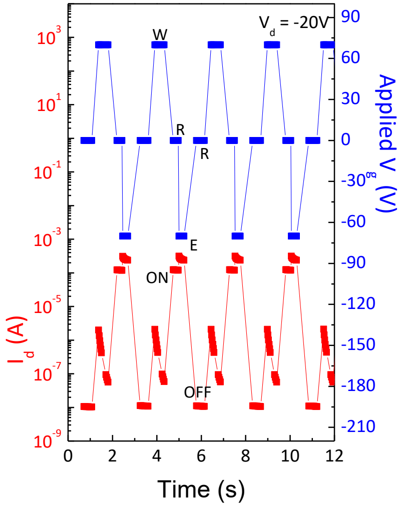
Organic Memory Transistors with One step synthesized Au NPs

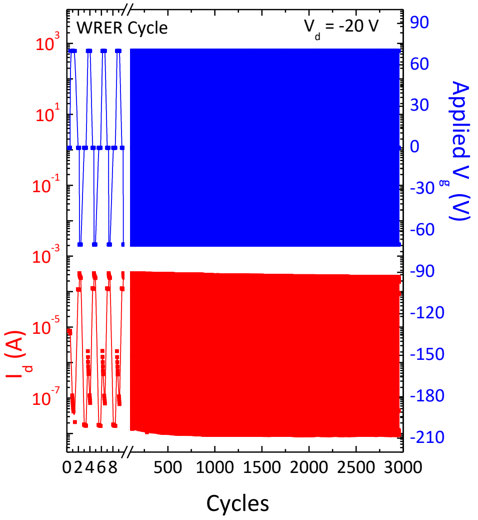
- Electrical characteristics

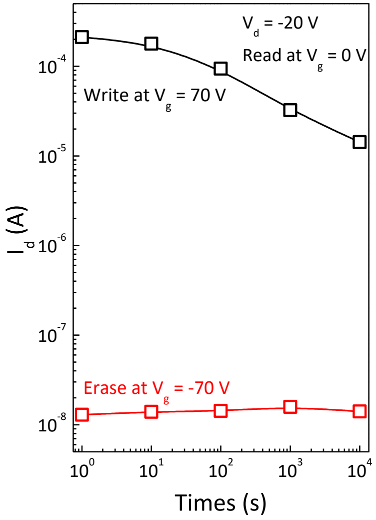










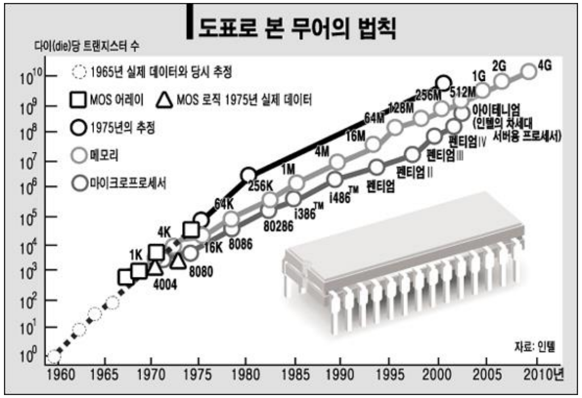


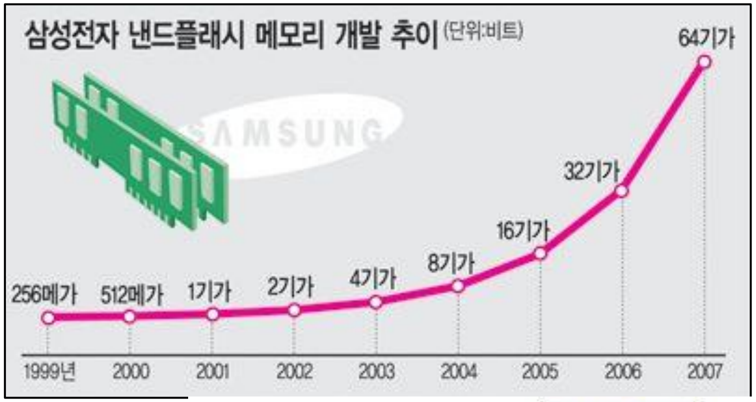
Neuromorphic Device

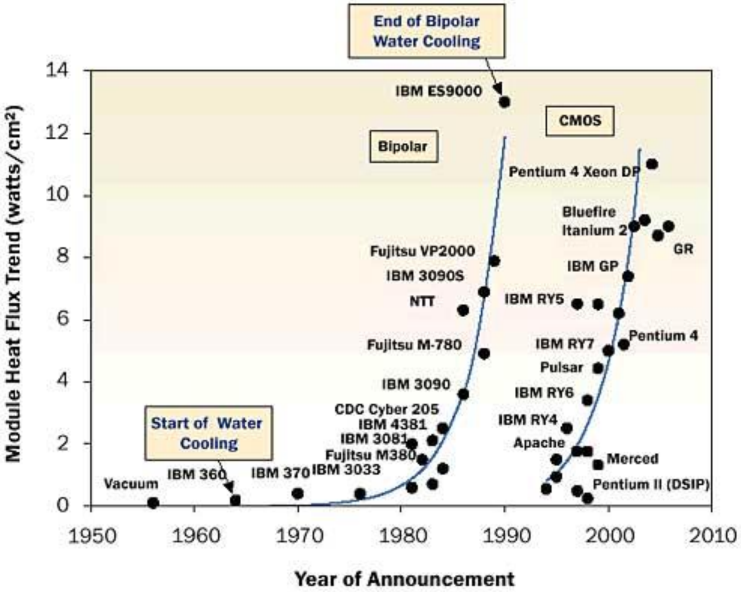
Ferroelectric Organic Neuromorphic Transistors (FONTs)

Why Neuromorphic Device?

무어의 법칙 (1965) : 반도체의 집적회로의 성능이 18개월 마다 2배씩 증가한다!
황의 법칙 (2002): 메모리 집적도가 1년에 두배 씩 늘어난다 !





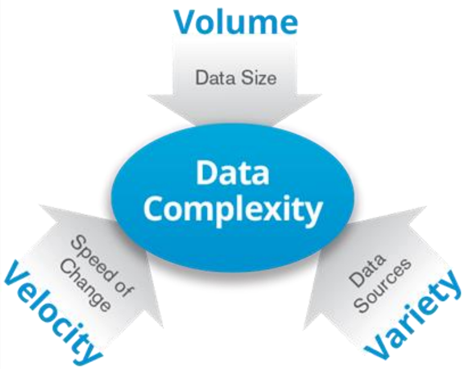


발열 문제?

Beyond CMOS → Neuromorphic chip

BIG DATA Era

- BIG DATA, Display, Electronic products, Genetic data, etc

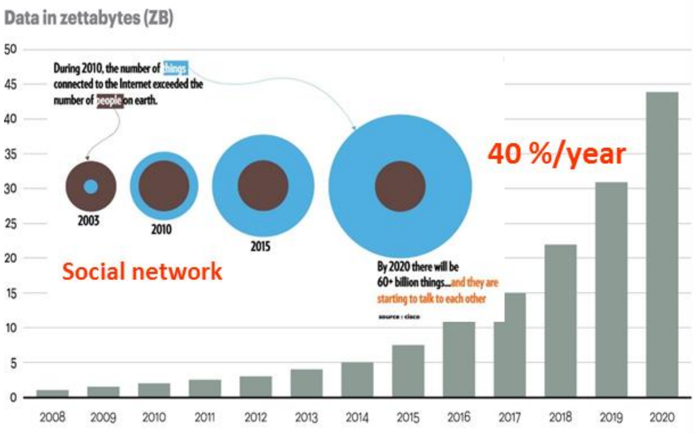


100 GB (for 4 k movie)
400 GB (for 8 k movie)

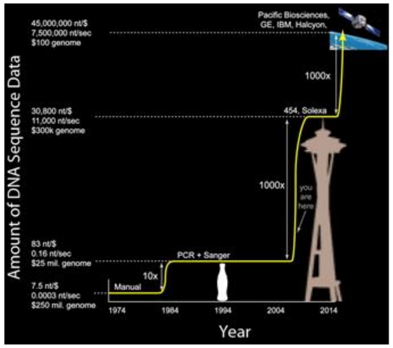
Google image

Figure 1

Data is growing at a 40 percent compound annual rate, reaching nearly 45 ZB by 2020

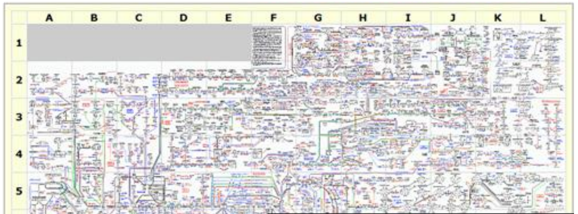


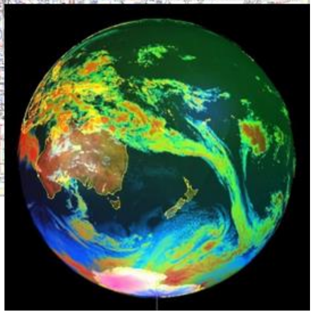
Source: Oracle, 2012



Genetic big data

Biochemical Pathways





Weather Big data

Heat, Energy Issues

- Storage, management, dissemination of organized information for business

Google data center world wide

Google Data Center

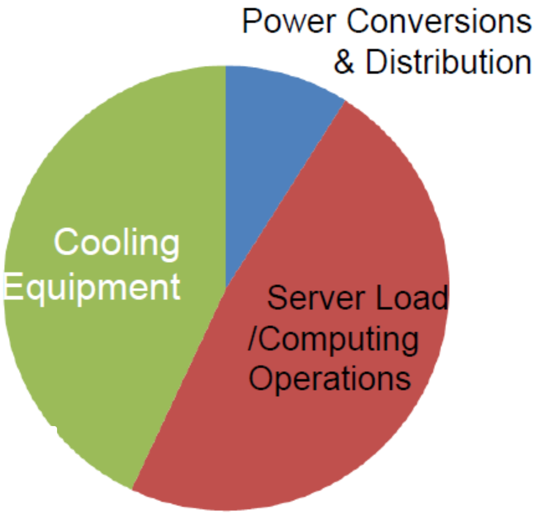
Trends in Data Center Energy Use (USA)

- ~ 100 billion kWh in 2011

Total amount of energy use (Korea, 2013-2014)

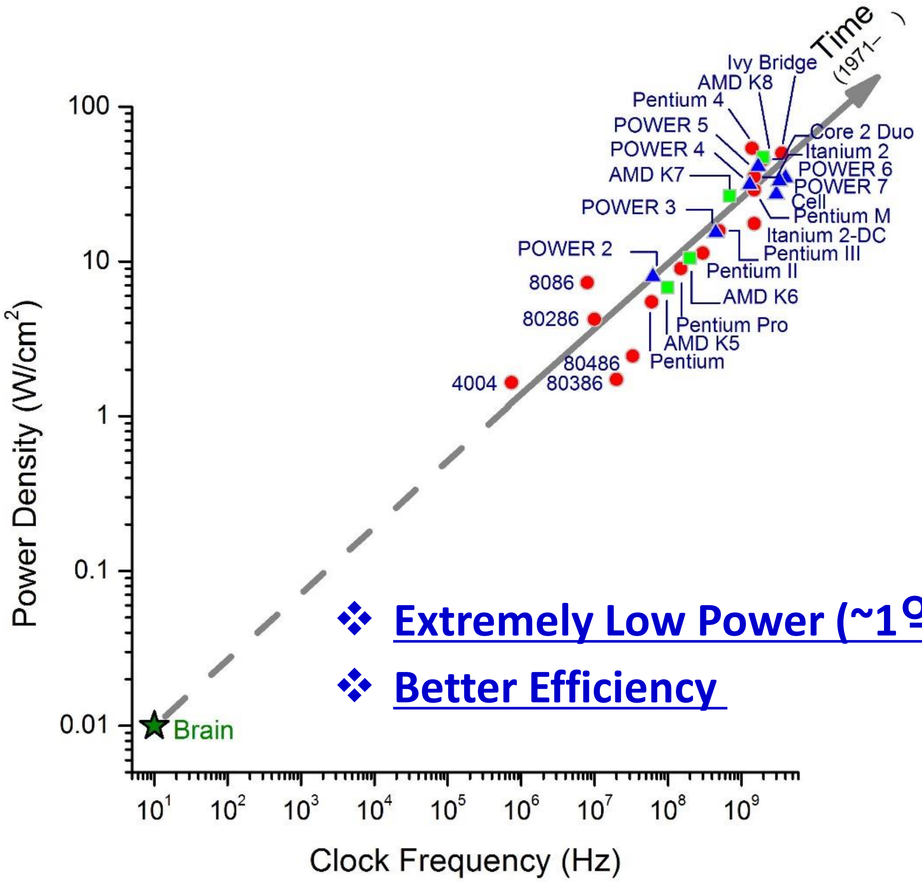
- ~ 100 billion kWh per year

Typical Data Center Energy End Use



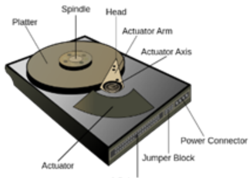
W. Tschudi, "Data Center Efficiency"

Why Brain mimicked Computer system?

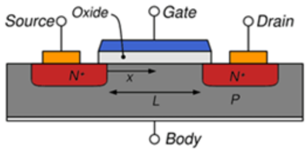


- **Extremely Low Power (~1억배)**
- **Better Efficiency**

Human Brain vs. Super Computer

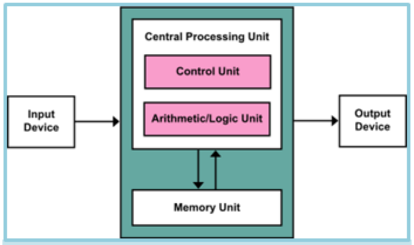


HDD

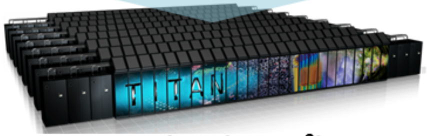


Si CMOS Transistor

Basic components



Von Neumann architecture



Titan (404 m^2)

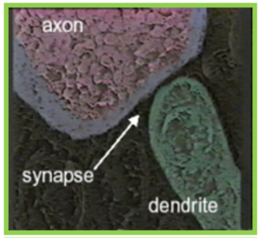
- 2 L
- 10^{11} neurons
- 10^{15} synapses
- 1-10 Hz (operational frequency)
- 20 W (power consumption)
- ~1 fJ (energy consumption)

1. Most efficiency computing system
2. Most complex system

(Potential # of synapses network >> ???)

- Super Computer (2nd ranked, Titan, 2012)'s CPU vs. Human Brain

Si CMOS Transistor (32 nm)	Basic device	Neuron (4 ~ 100 μm) Synapse (~ 100 nm)
~ 200 x 10^{12} CMOS transistors ~ 19 K (CPU + GPU)	# of device	~ 10^{11} Neurons ~ 10^{15} Synapses
~20 x 10^{15} FLOPS	Computational power	> 40 x 10^{15} FLOPS
8.2 x 10^6 W	Power	20 W
Programmed, fast numerical cal., serial/parallel processing	Remarks	Learning, massively parallel signal processing



Synapses

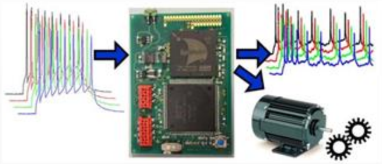
Neuron

Human brain

Status of Current Research on Neuromorphic Devices

Proposal 영국 멘체스터 대학 SpiNNaker

- 다중채널 spiking input/output
- Simulates ~20,000 neurons
- 20 x 20 mm, 60 mW



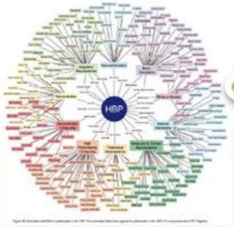
SpiNNaker
Biologically
Inspired
Massively
Parallel
Architectures

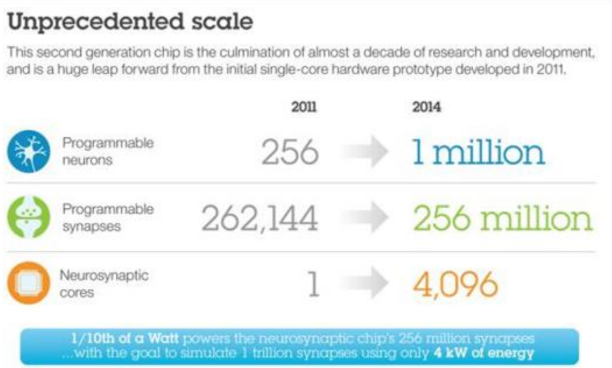
MANCHESTER
1824

Proposal 유럽의 Human Brain Project (1조 7천억)

- Neuroscience (뇌 시뮬레이션)
- 뇌 질환 관련 의료 분야
- 뇌 모사 인지 컴퓨팅

Human Brain Project





Unprecedented scale

This second generation chip is the culmination of almost a decade of research and development, and is a huge leap forward from the initial single-core hardware prototype developed in 2011.

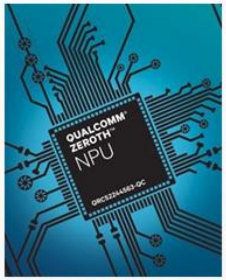
	2011		2014
Programmable neurons	256	→	1 million
Programmable synapses	262,144	→	256 million
Neurosynaptic cores	1	→	4,096

1/10th of a Watt powers the neurosynaptic chip's 256 million synapses ...with the goal to simulate 1 trillion synapses using only **4 kW of energy**

Proposal 기업 주도 성취 (미국)

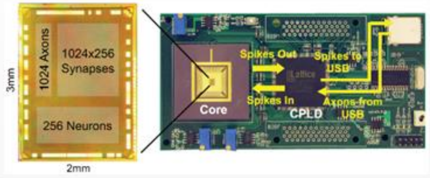
- **IBM TruNorth chip (2014)**, 2 억 5천만 개의 시냅스 (54 억개의 Tr.) → **보행자, 차량 구별 시연**

- **Qualcomm Zeroth Program** 모바일 프로세스와 연결 가능한 NPU (뉴로시냅틱 HW) 개발 → **자율 주행 로봇 시연**



Proposal 미국 DARPA의 SyNAPSE 프로그램

- 뇌 모방형 칩 개발
- 뇌 모방형 아키텍처 설계
- 시스템 시뮬레이터 개발

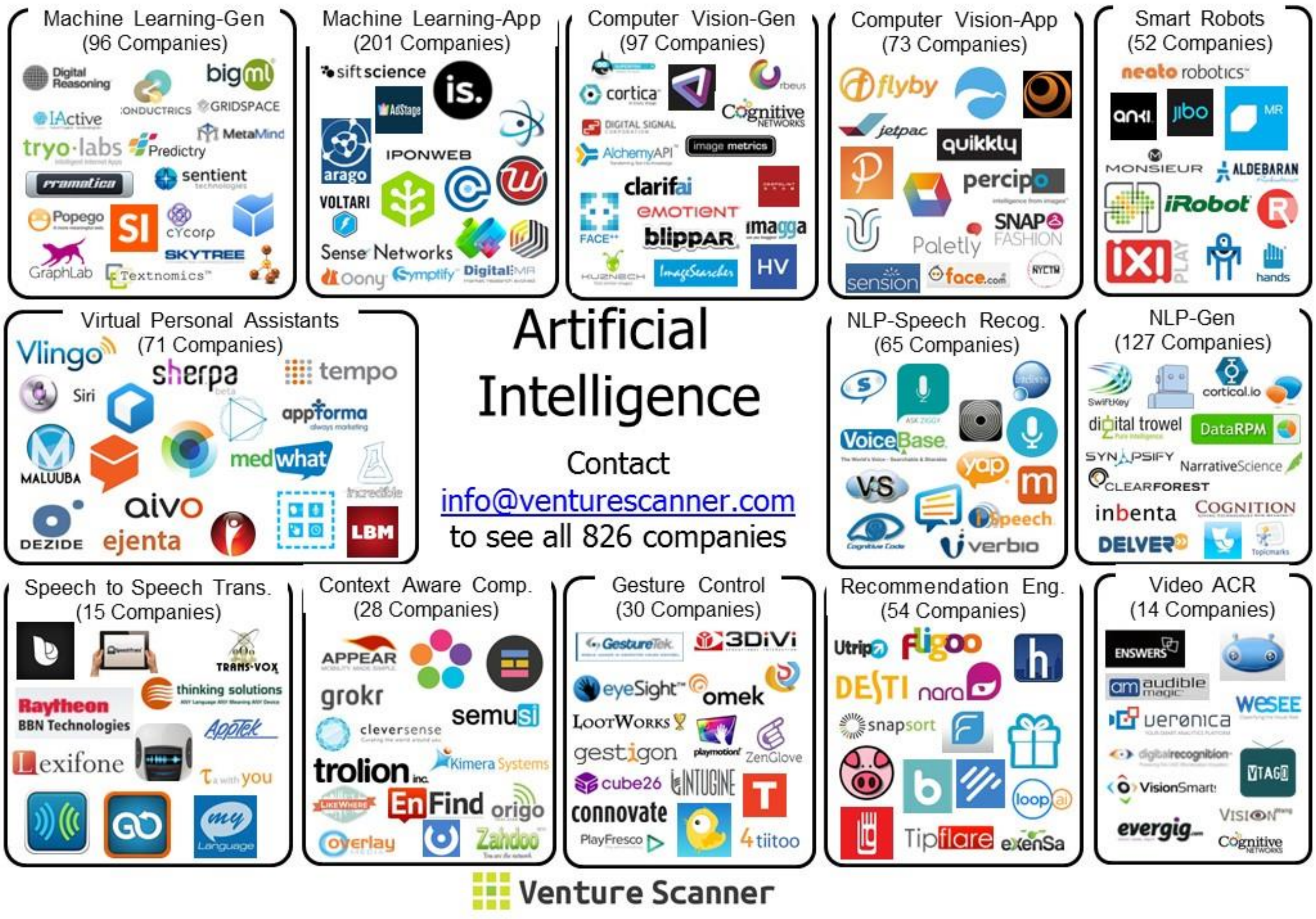


SyNAPSE

IBM

HRL LABORATORIES

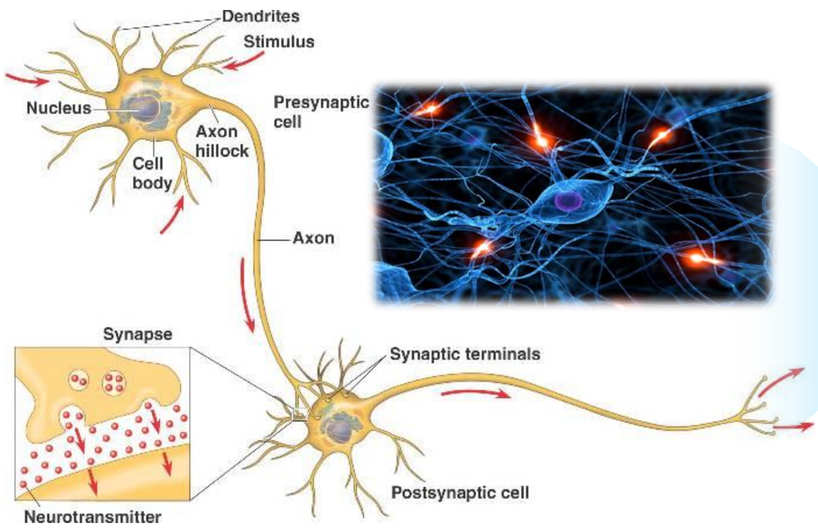
Status of Current Research on Neuromorphic Devices



Contact info@venturescanner.com to see all 826 companies

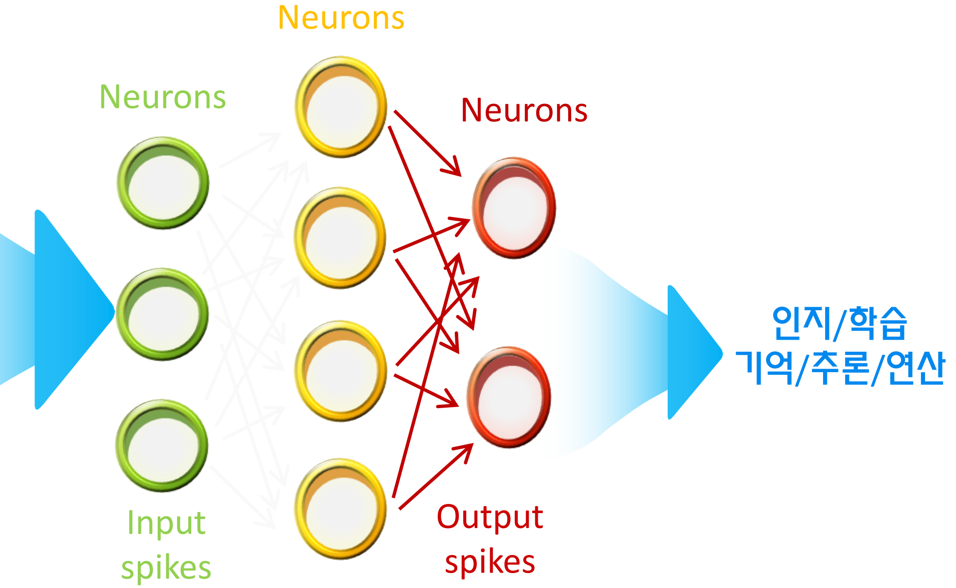
Neuron

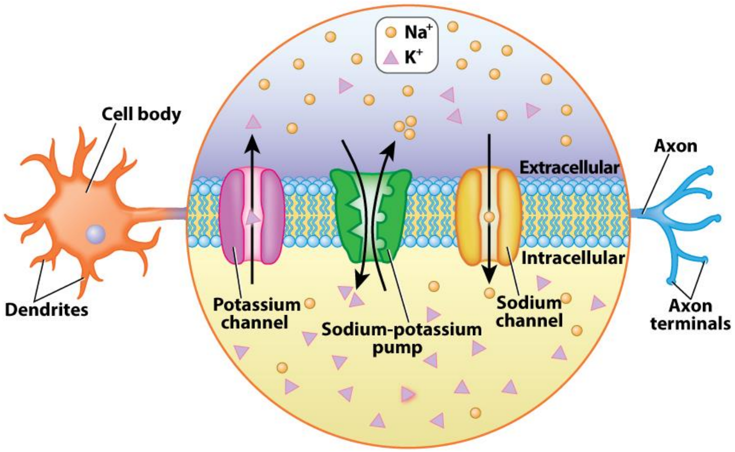
Neuron and synapse

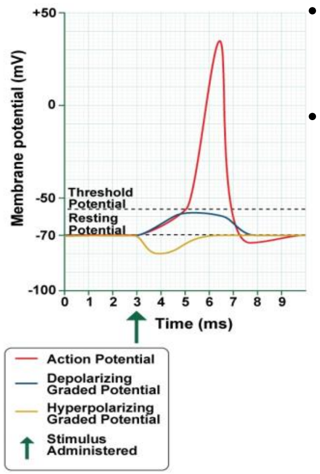


~10^3 시냅스/뉴런

Parallel network



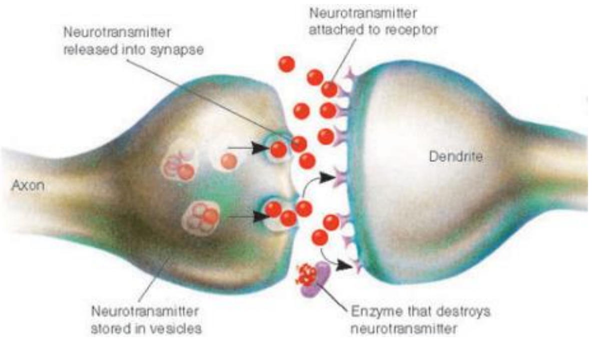




- Small changes in membrane potential (graded potentials) can be depolarizing or hyperpolarizing.
- A depolarizing potential that exceeds a threshold becomes an action potential.

Synaptic Plasticity

Synaptic plasticity is the ability of synapses to strengthen or weaken over time, in response to increases or decreases in their activity. (**기억,학습,연산,추론과 관련된 기능**)
Memory, learning, computation, reasoning



Excitatory vs. Inhibitory Synapse

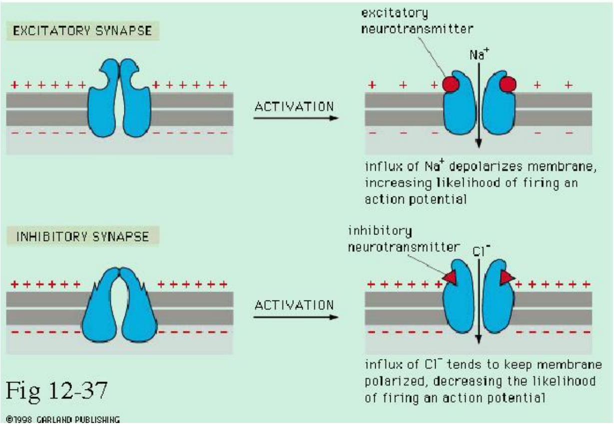


Fig 12-37

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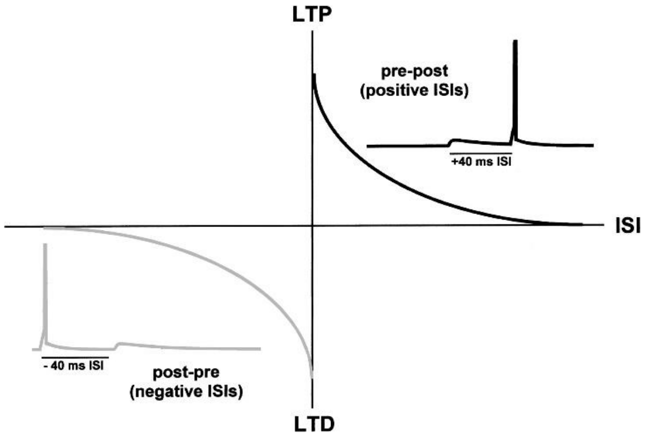
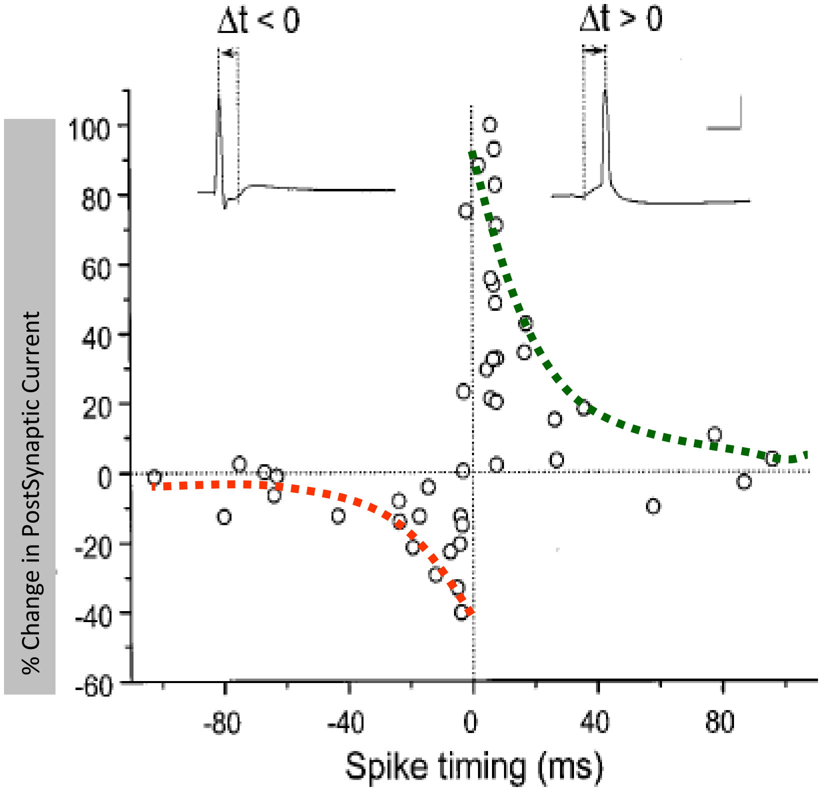
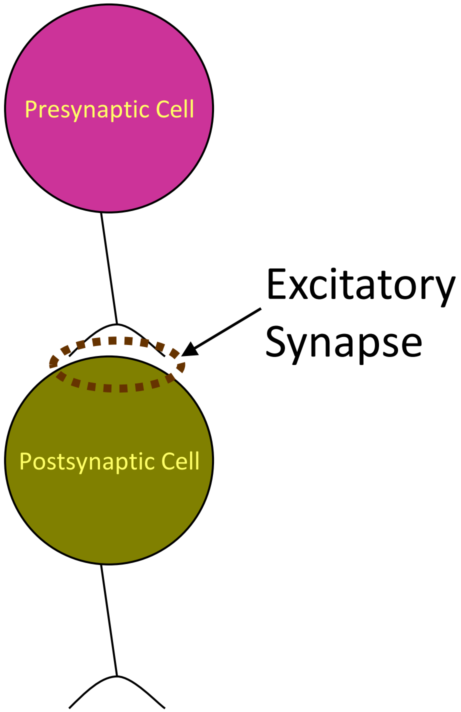
Hebb’s Postulate: When an axon of cell A... excites cell B and repeatedly or persistently takes part in firing it, some growth process or metabolic change takes place in one or both cells so that A's efficiency as one of the cells firing B is increased.



In standard Hebbian learning, a synaptic weight is increased if presynaptic and postsynaptic neuron are `simultaneously' active. If neurons communicate by spikes, the concept of simultaneity implies the pre- and postsynaptic spikes occur within some time window. Theory predicts that these time windows could have two phases corresponding to an increase (potentitiation) or decrease (depresseion) of the synaptic weight depending on the relative timing of pre- and postsynaptic spike. Such asymmetric learning rules with two phases have been found in recent experiments.

Spike Timing Dependent Plasticity (STDP)




Presynaptic Cell

Excitatory Synapse

Postsynaptic Cell

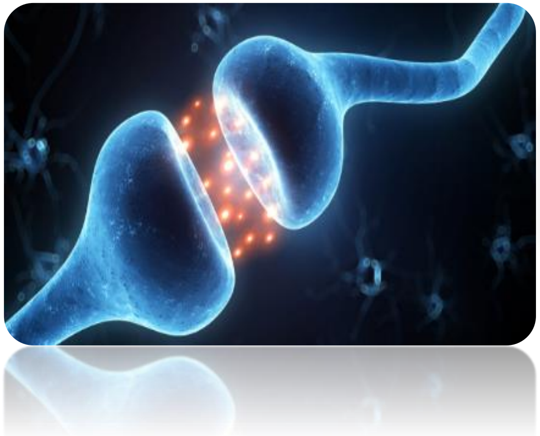
$$\Delta t = t_{post} - t_{pre}$$

Guo-qiang Bi and Mu-ming Poo, J. of Neuroscience, December 1998

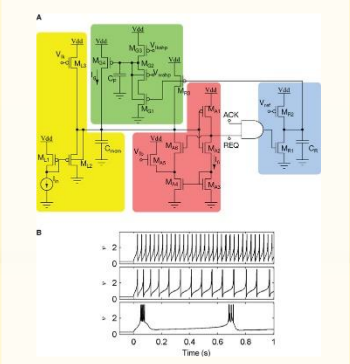
Mimicking Synaptic Device

- ■ **Long Term Potentiation (LTP), Long Term Depression (LTD) (장기기억, 학습)**
- ■ **STP, STD (for Short Term Memory)**
- ■ **Spike Timing Dependent Plasticity (STDP)**
- ■ **Ultralow power**
- ■ **Ultrahigh density**
- ■ **…**

■ **Function of synapse**

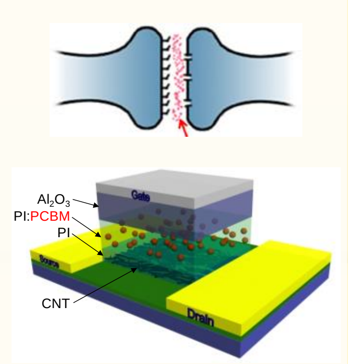


Analog Tr neuromorphic circuit



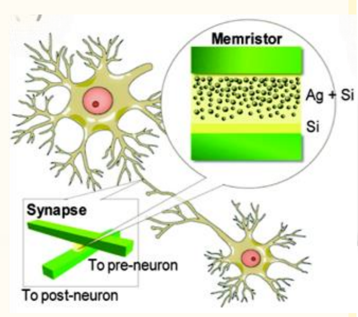
***Front. Neurosci.**, (2011)*

Floating-gate synaptic device



Small, (2013)

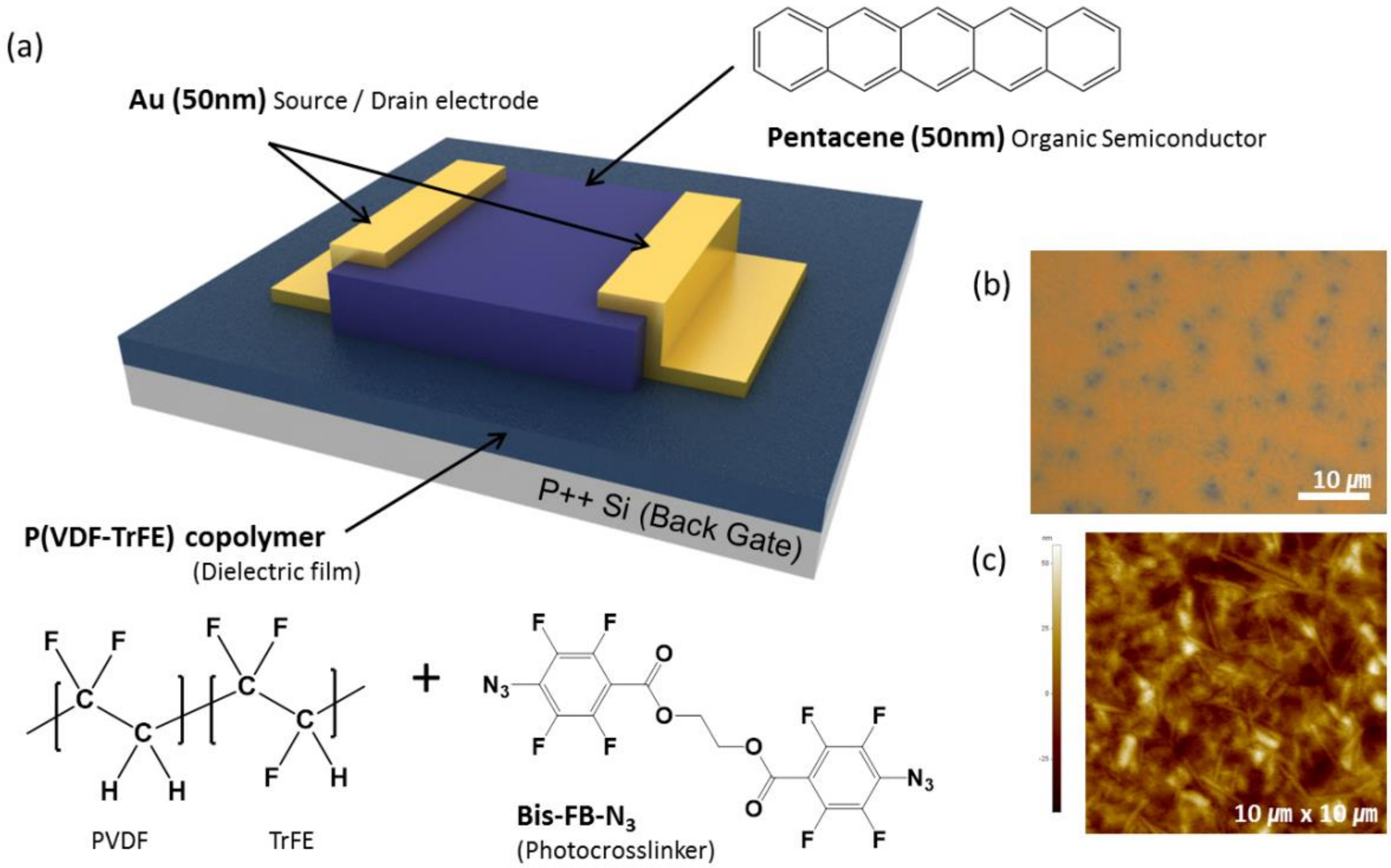
Resistive/memristor synaptic device



Nano Letters, (2010)

Control of ferroelectricity of P(VDF-TrFE)

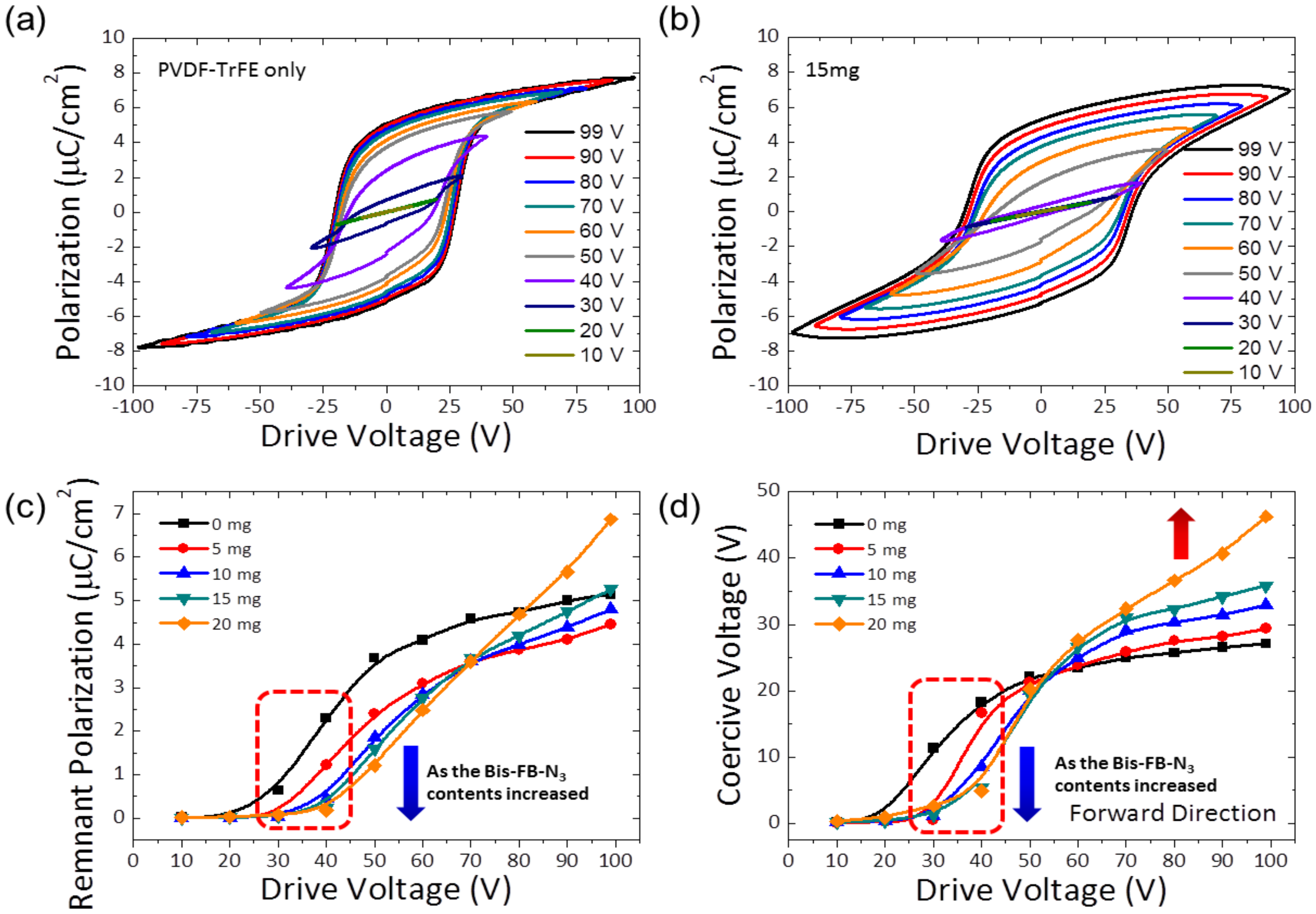
- Device structure and materials



Jang et al, Manuscript in preparation (2017)

Control of ferroelectricity of P(VDF-TrFE)

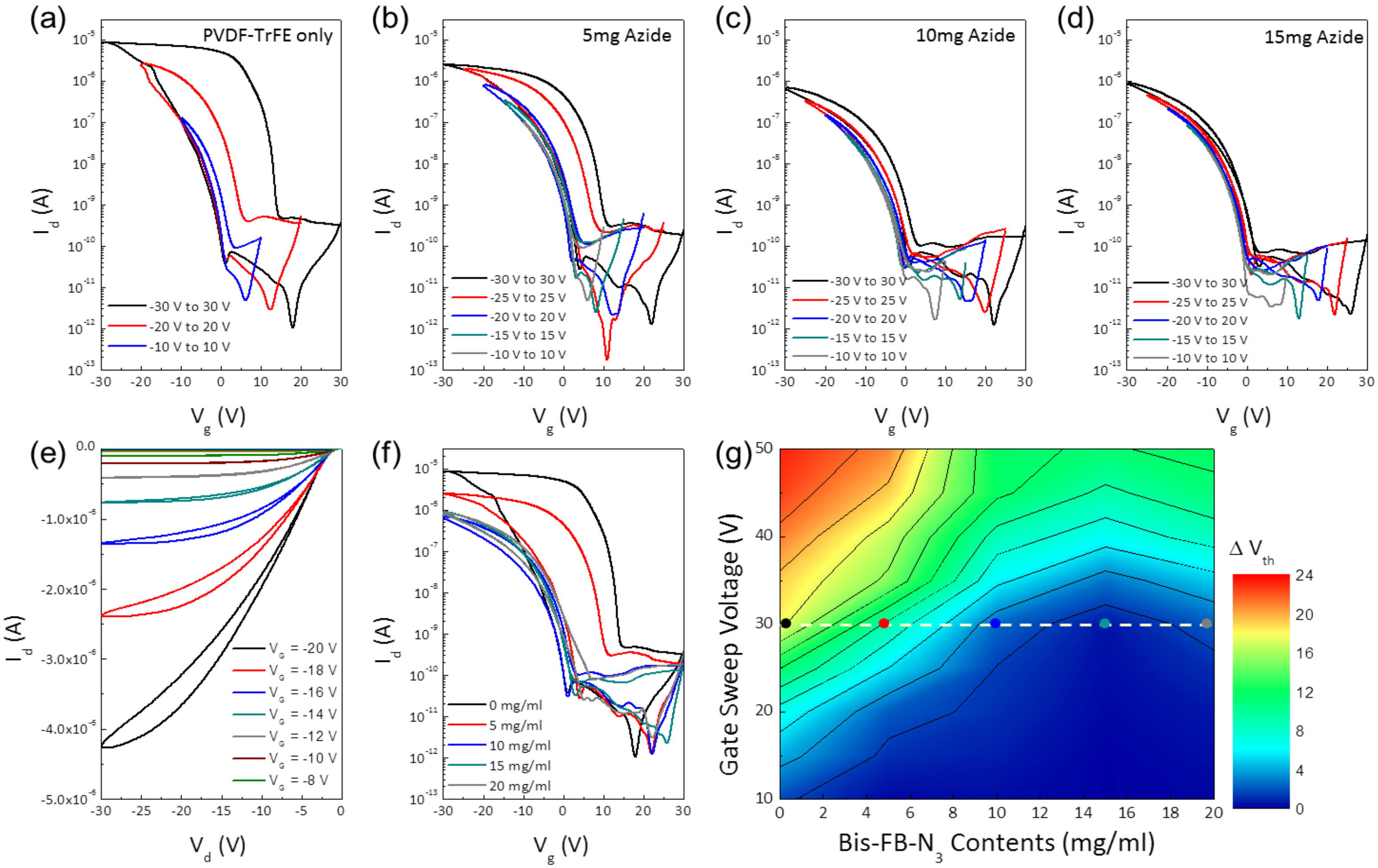
- Polarization curve via contents of crosslinker



Jang et al, Manuscript in preparation (2017)

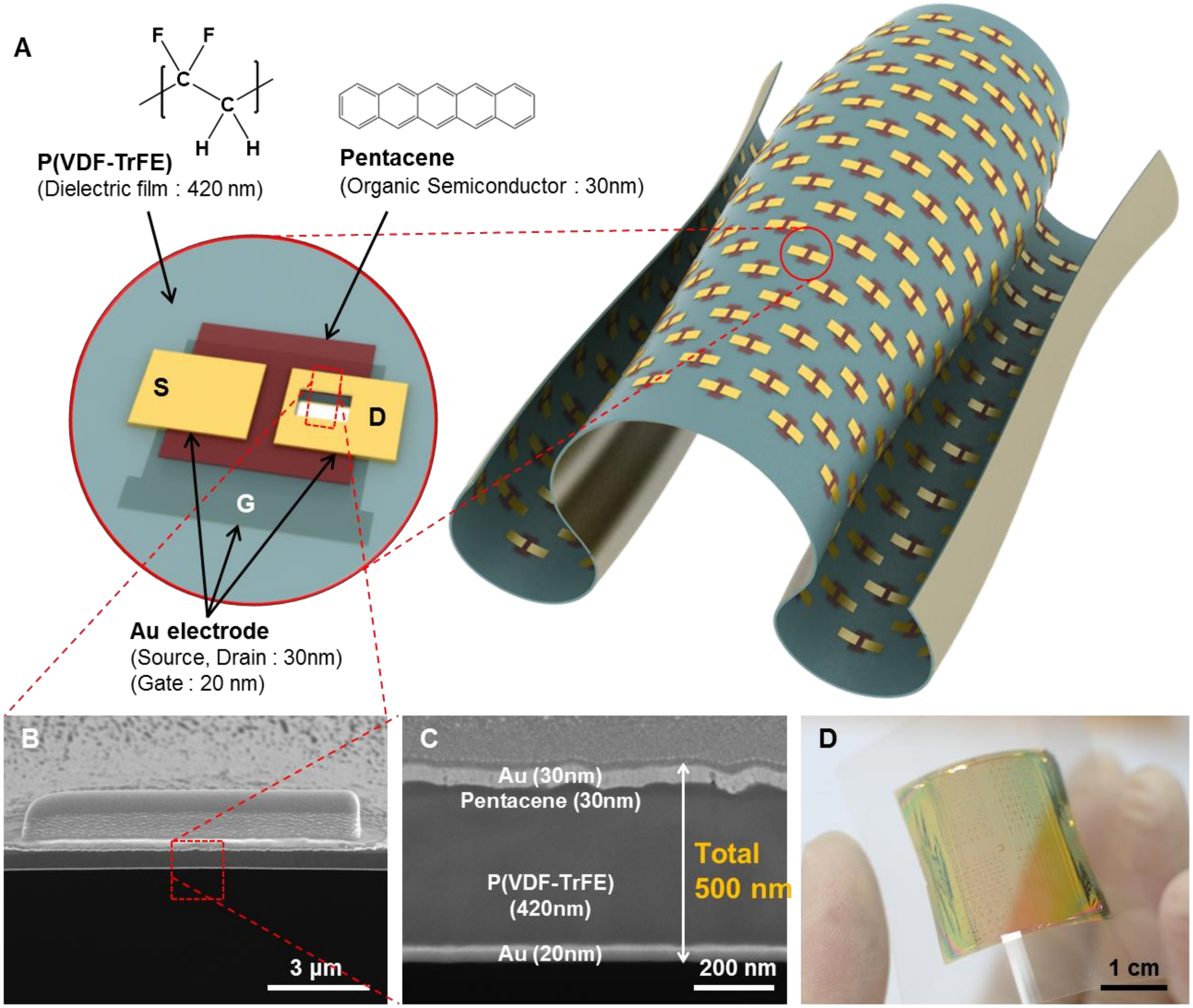
Control of ferroelectricity of P(VDF-TrFE)

- Transfer curves of the ferroelectric transistors via contents of crosslinker



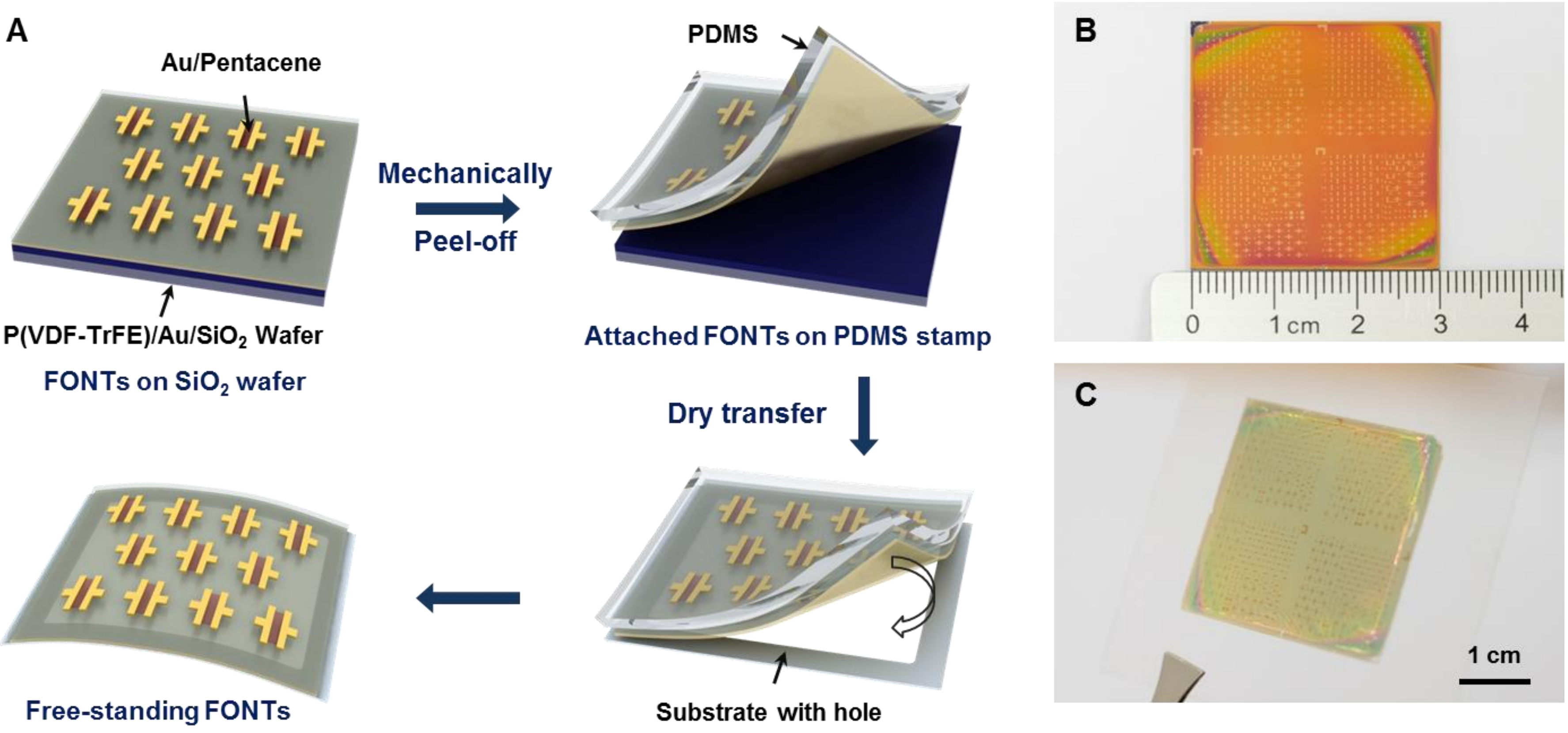
Jang et al, Manuscript in preparation (2017)

Ferroelectric organic neuromorphic transistors (FONTs)

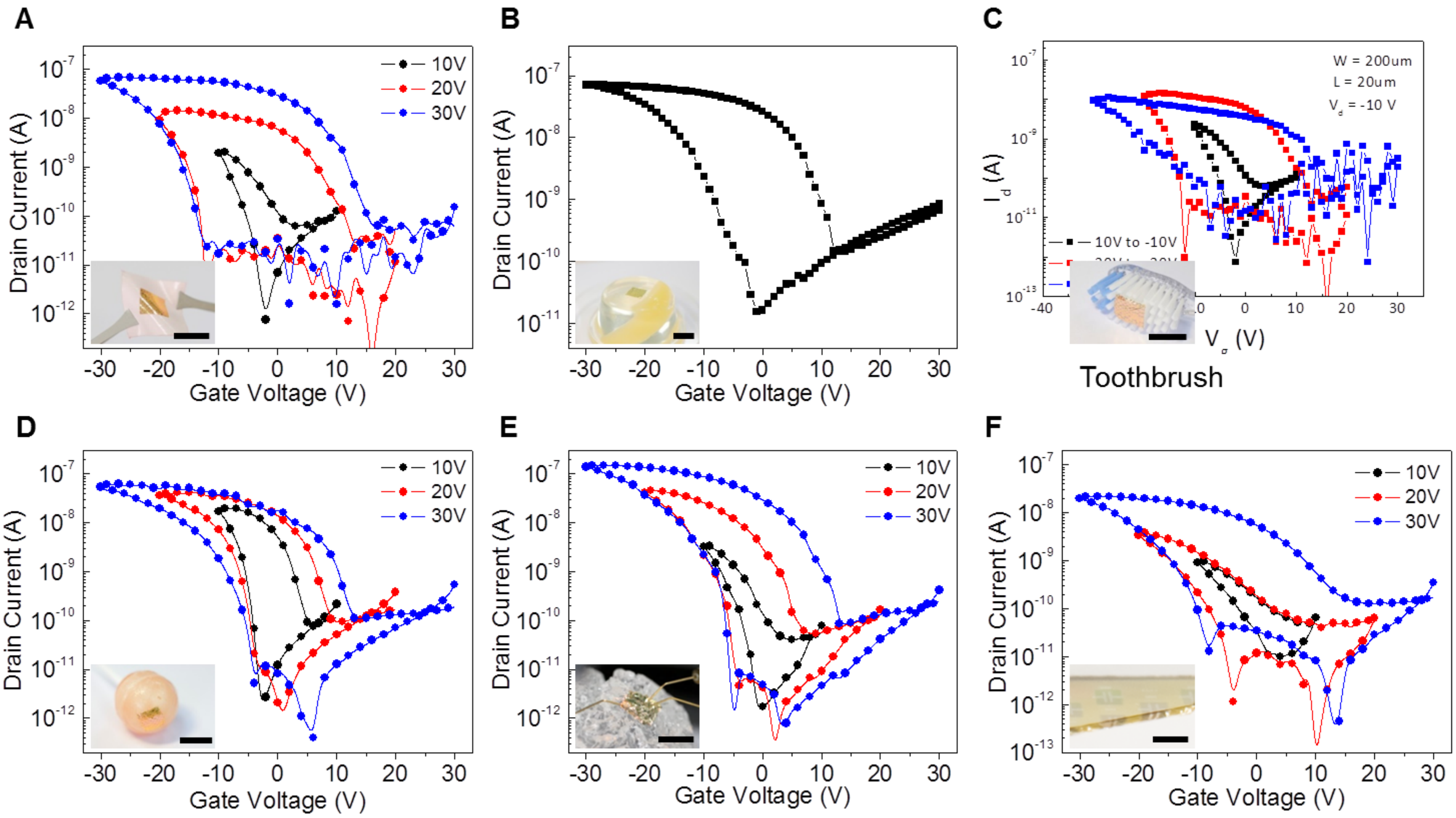


Jang et al, In revision (2018)

Ferroelectric organic neuromorphic transistors (FONTs)

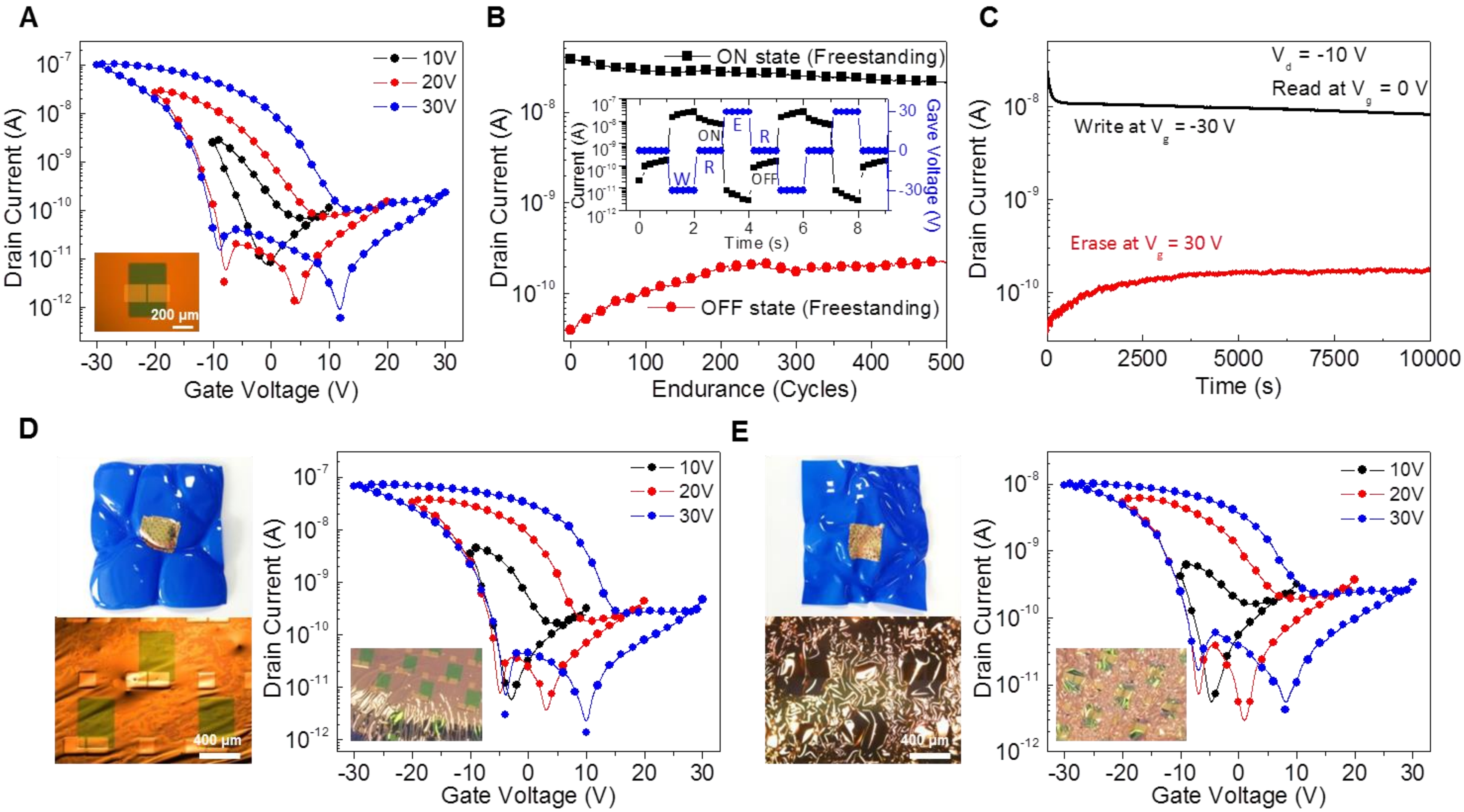


Ferroelectric organic neuromorphic transistors (FONTs)



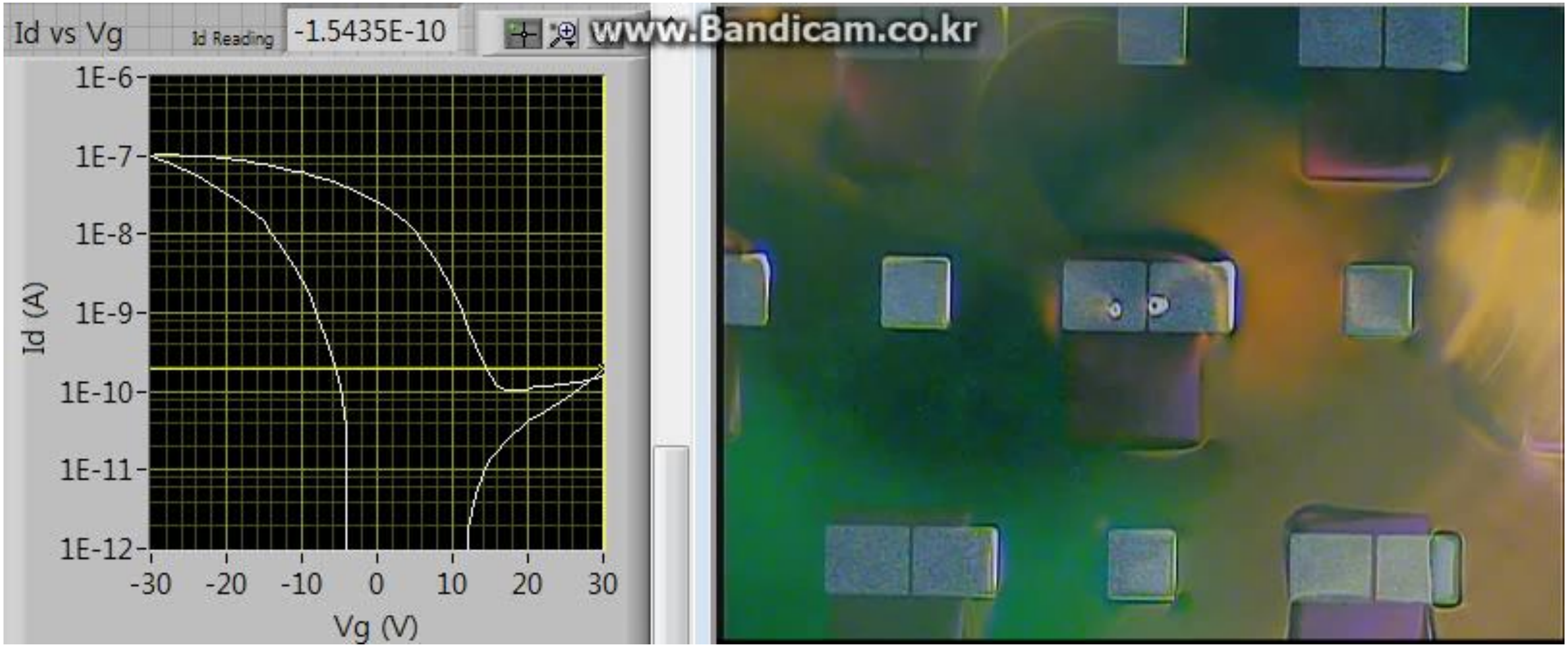
Toothbrush

Ferroelectric organic neuromorphic transistors (FONTs)

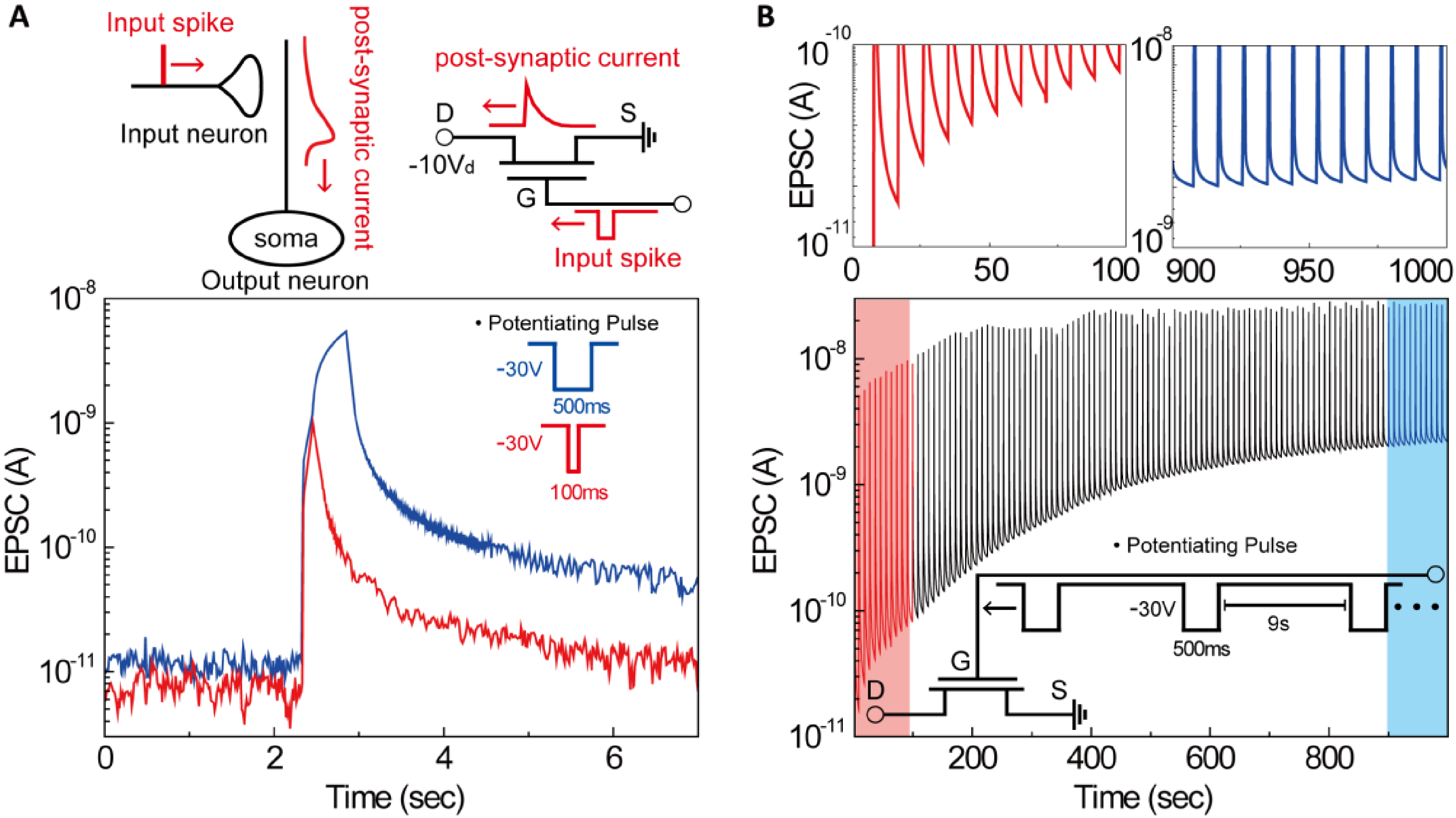


Ferroelectric organic neuromorphic transistors (FONTs)

- Video of I-V characteristics of Free-standing Ferroelectric organic neuromorphic transistors (FONTs)

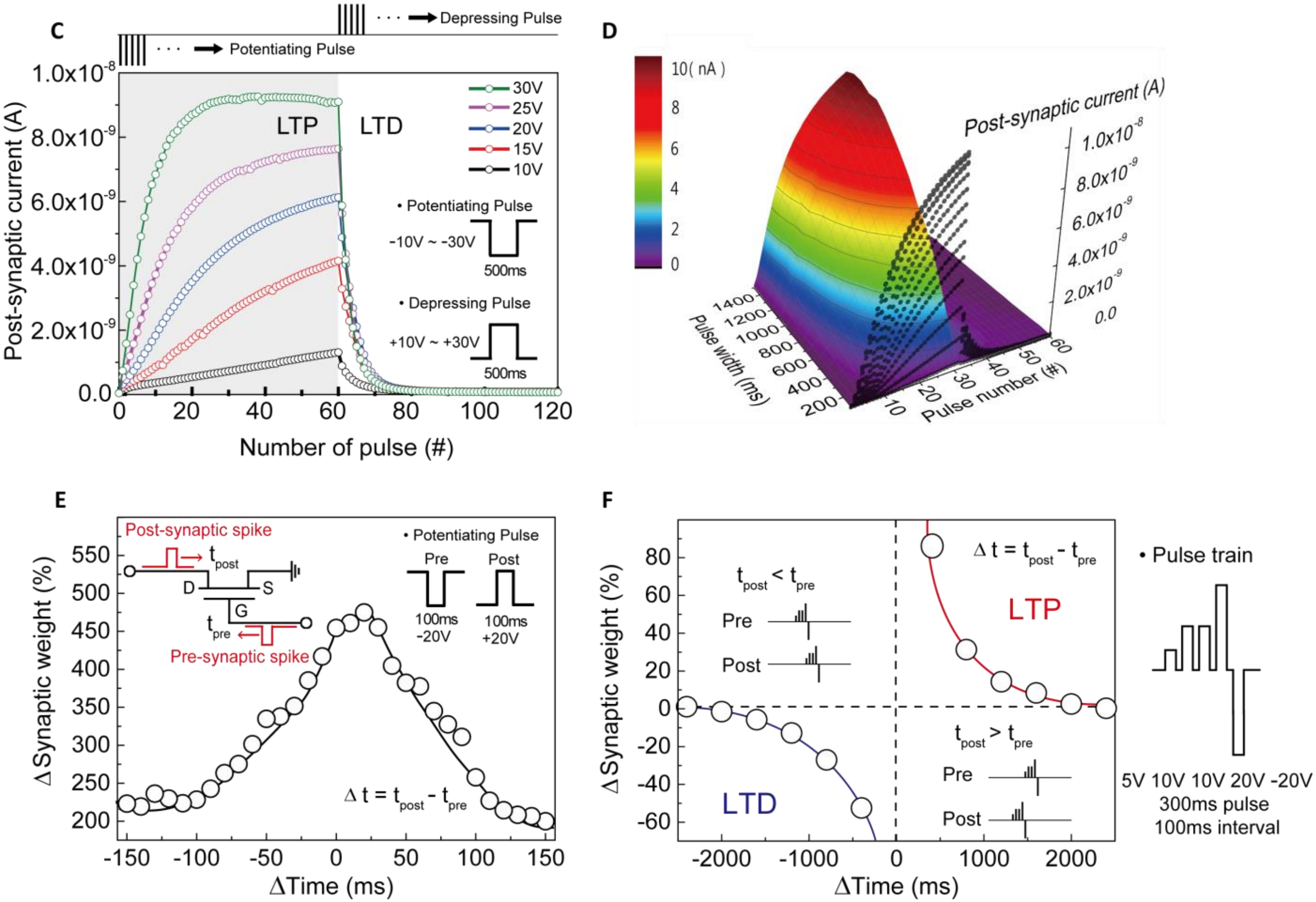


Ferroelectric organic neuromorphic transistors (FONTs)

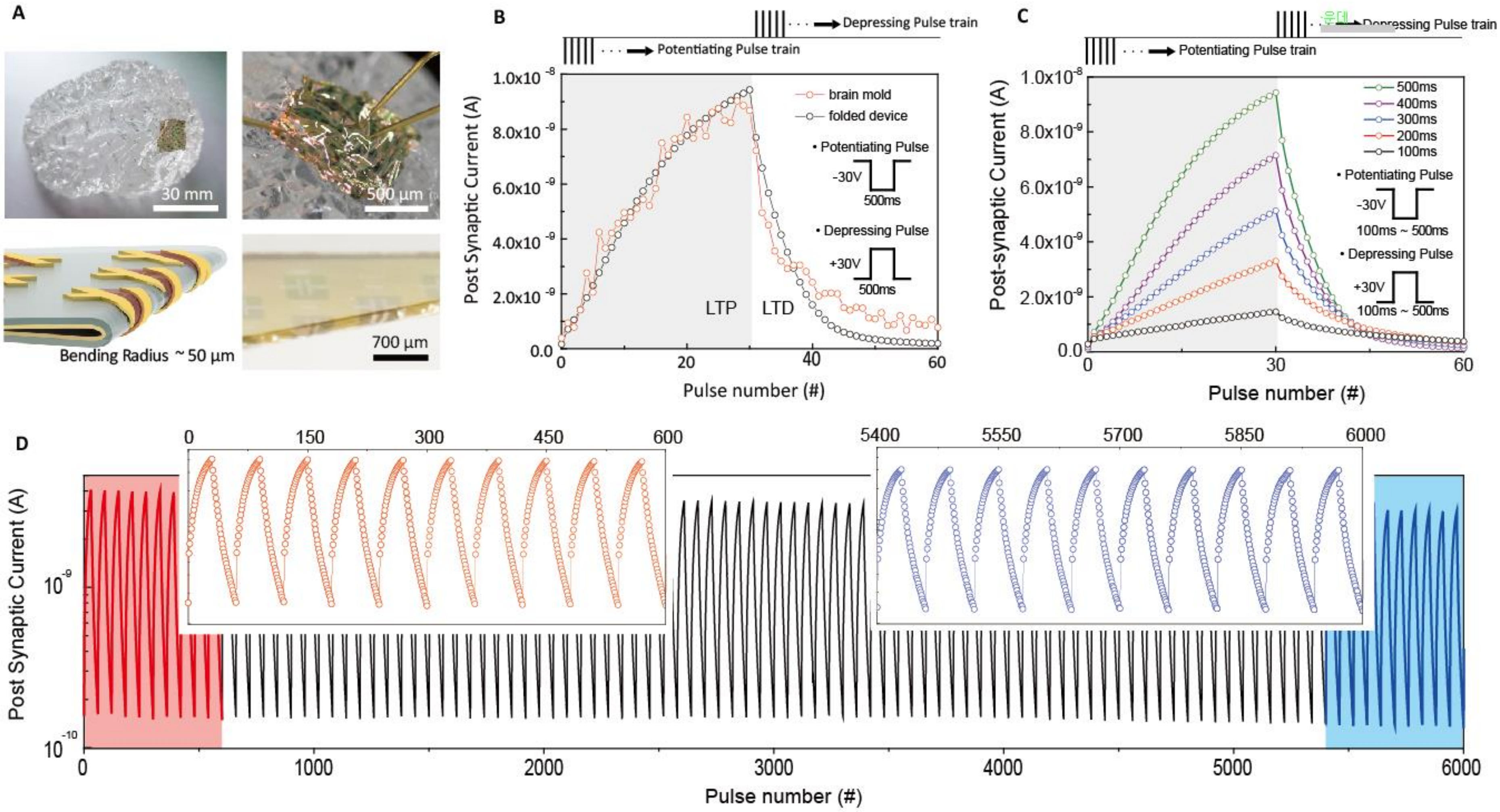


Jang et al, In revision (2018)

Ferroelectric organic neuromorphic transistors (FONTs)



Ferroelectric organic neuromorphic transistors (FONTs)



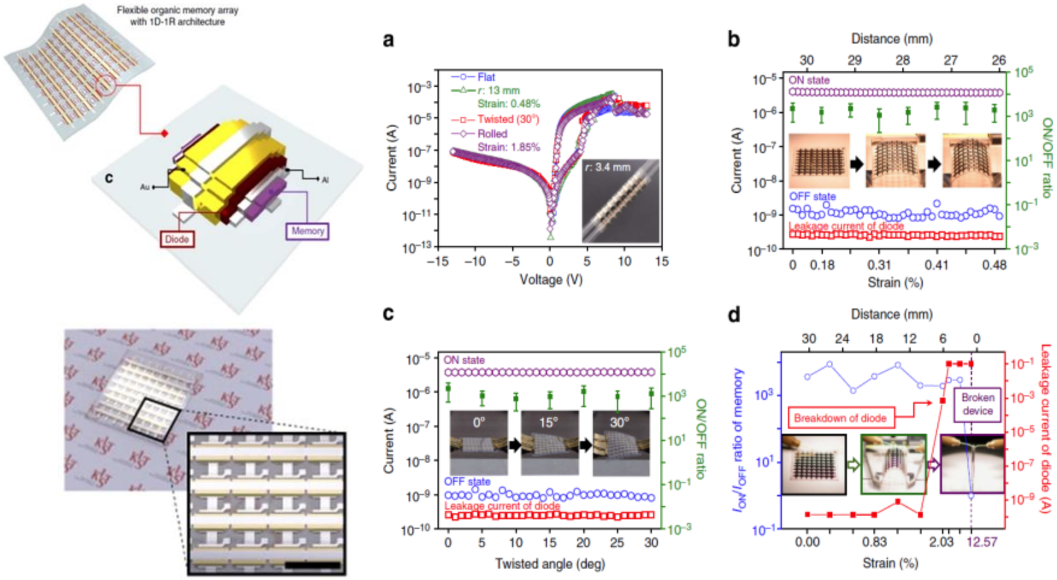
Jang et al, In revision (2018)

Next-generation Wearable Device Platform

Fibriform Organic Memory Transistors

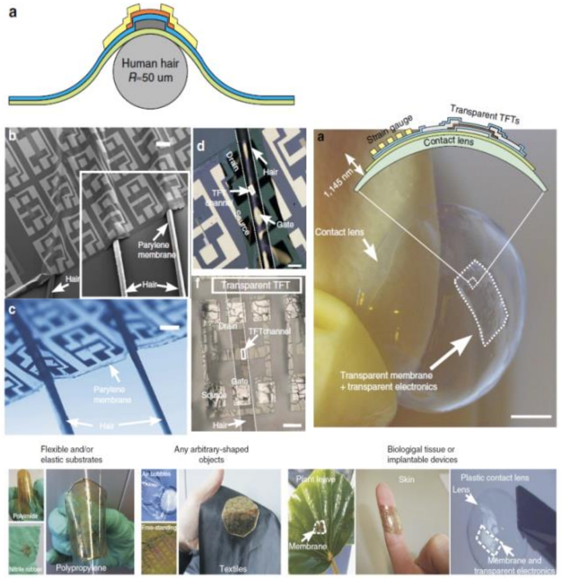
Previous Research on Flexible Devices

- Flexible, Twistable, Rollable memory



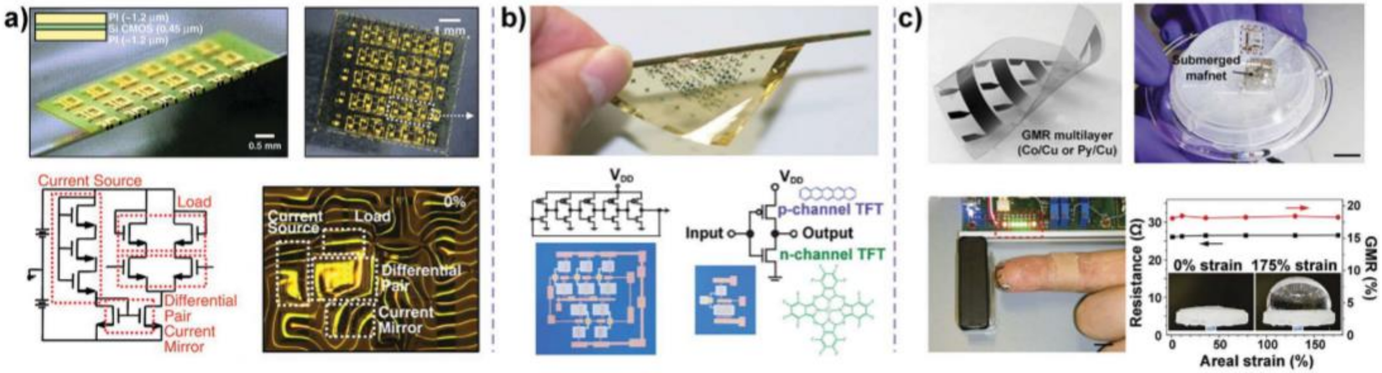
Nature Comm., 4, 2707 (2013)

- Flexible Transferable device



Nature Comm., 5, 2982 (2014)

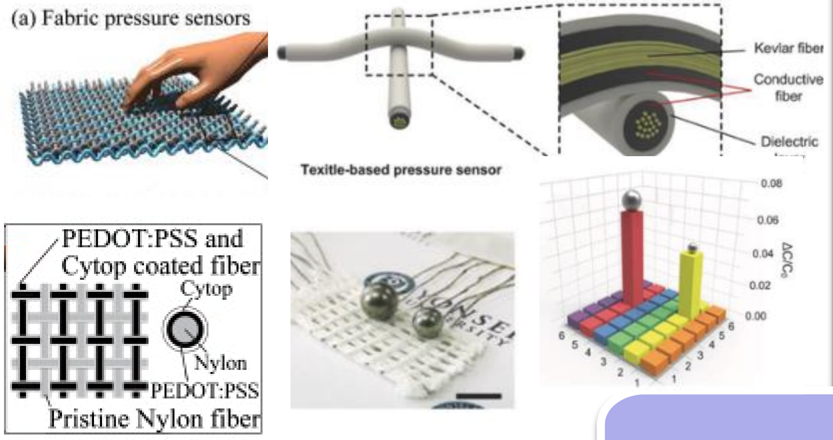
- Stretchable, Rollable electronic circuit on flexible substrate



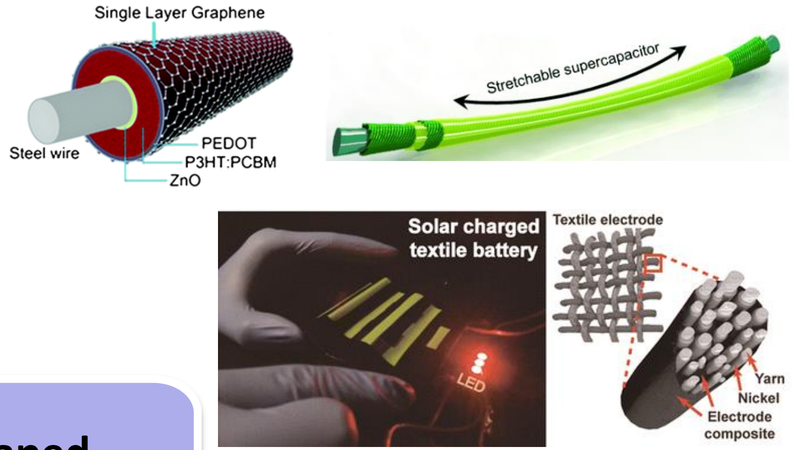
Science, 320, 507 (2008)
Nat. Mater., 9, 1015 (2010)
Nat. Commun. 6, 6080 (2015)

Fiber-Shaped Electronic Devices

Sensors

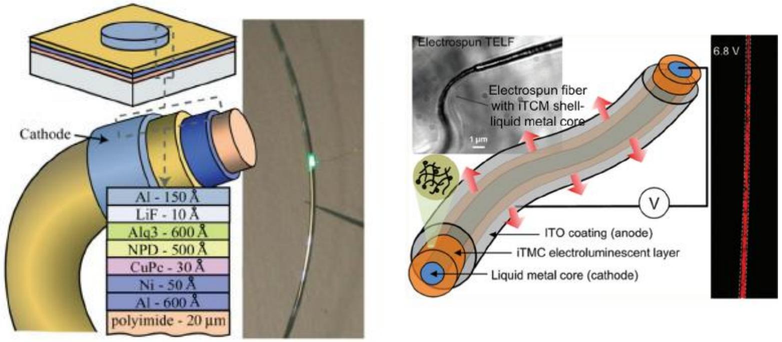


Energy devices

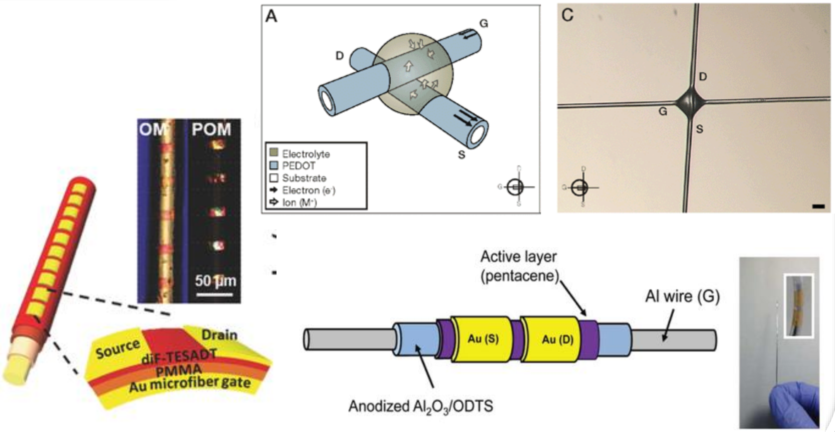


Fiber-shaped electronic devices

Light-emitting diode

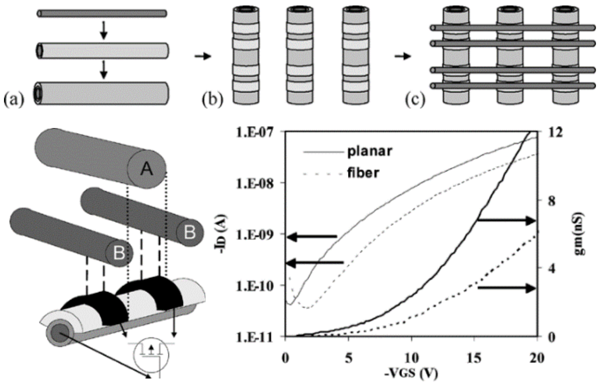


Transistors & Memories



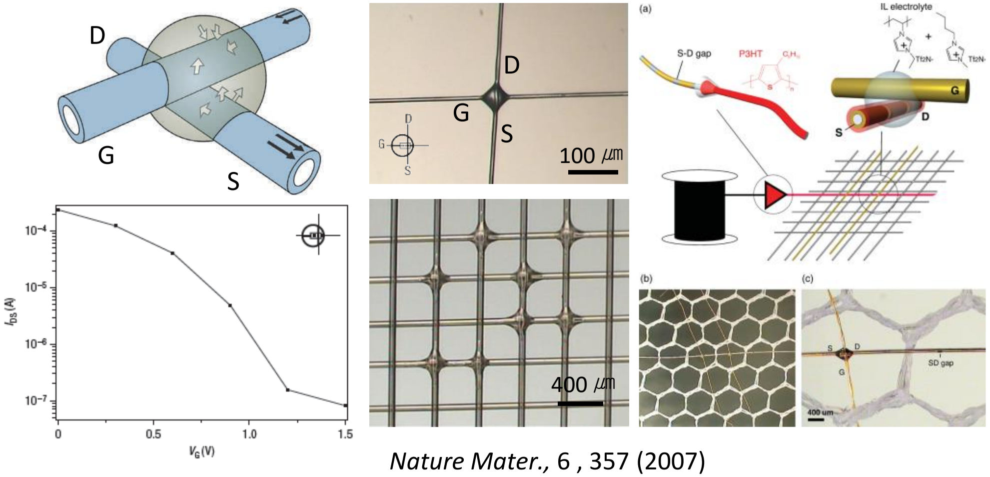
Previous Research on Fiber-type Electronic Devices

Weaved OTFT on Fiber



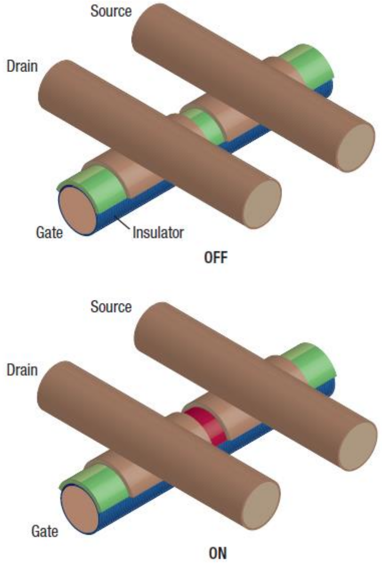
IEEE Trans. Electron Dev., 52, 269 (2005)

Wire Electrochemical Transistors (WECTs)

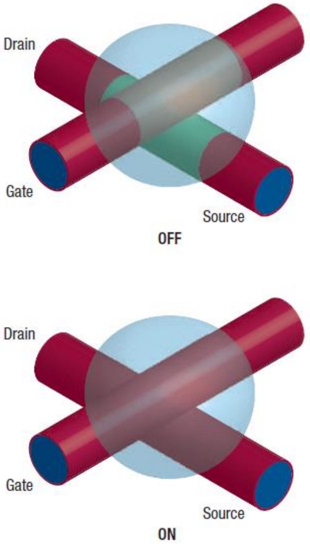


Nature Mater., 6 , 357 (2007)
Adv. Mater., 21, 573 (2009)

Fiber OFET



WECT



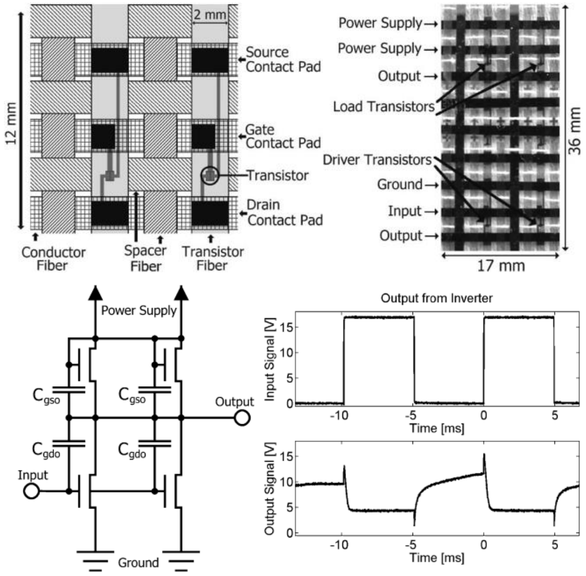
- 🟦 Insulator
- 🟫 Conductor
- 🟩 Semiconductor in the low-conduction state
- 🟥 Semiconductor in the high-conduction state
- 🟦 Ion reservoir

Nature Mater., 6 , 328 (2007)
Adv. Mater., 26, 5310 (2014)

Category	Fiber OFET	WECT
Mobility	>0.5 $cm^2\ V^{-1}\ s^{-1}$[76]	Very low
	Up to 1.4 $cm^2\ V^{-1}\ s^{-1}$	
Operating voltages	About 9–20 V	0–1.5 V
On/off ratio	10^3–10^5	10^2–10^3

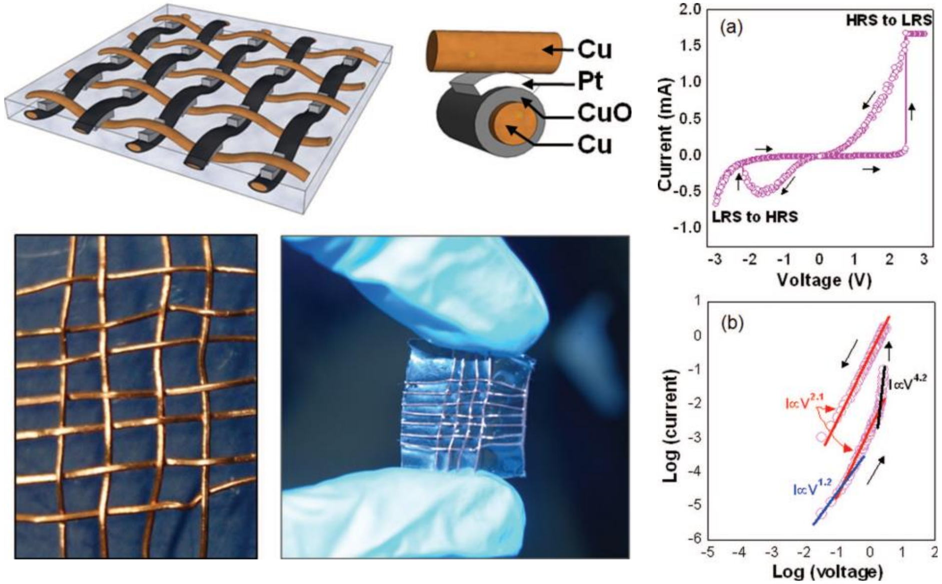
Previous Research on Fiber-type Electronic Devices

- Woven Inverter circuit



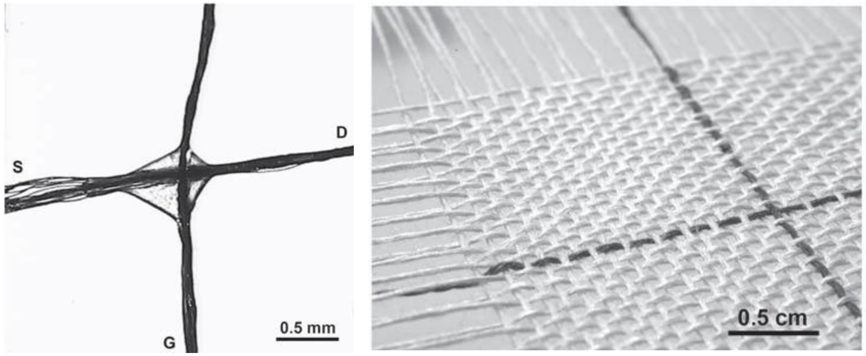
IEEE EDL, 25, 295 (2004)

- Woven Resistive Memory Array



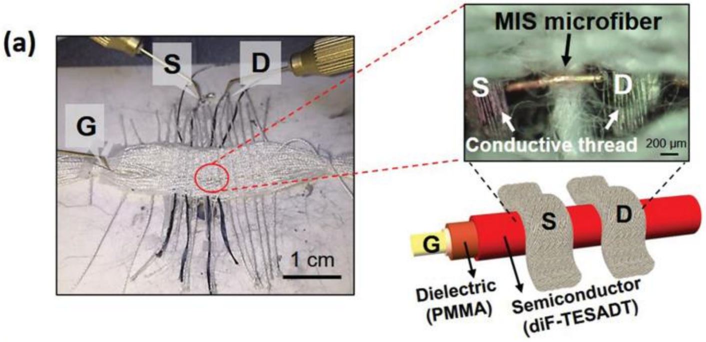
AIP Advances 1, 032162 (2011)

- Weaving with silk fabric



Adv. Mater., 23, 898 (2011)

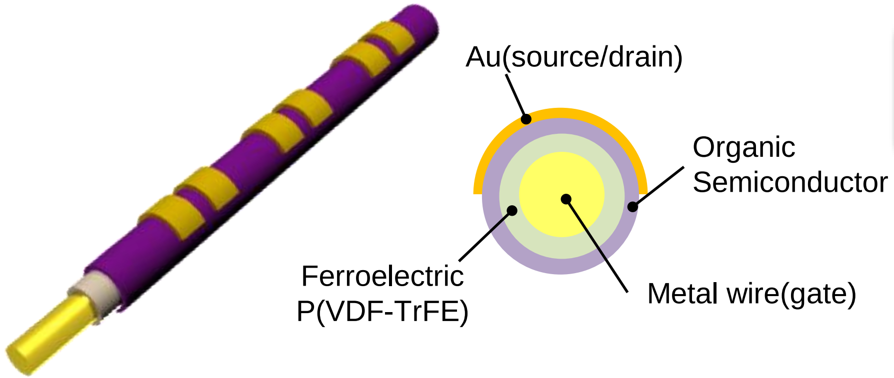
- Fibriform OFET embedded in the textile



Adv. Funct. Mater. 26, 2706 (2016)

Fiber-Shaped Organic Ferroelectric Memory Transistors

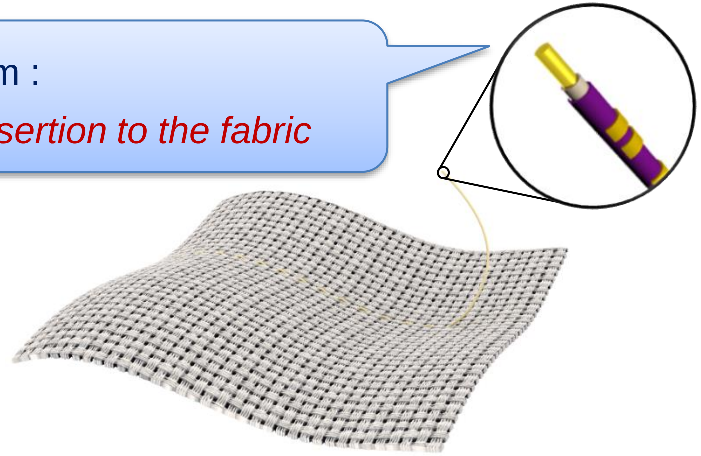
Target : 1-D memory transistors on single fiber



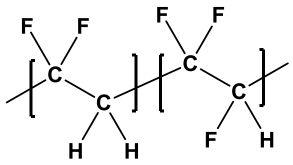
Fiber-shaped organic ferroelectric memory transistor

Final aim :

Fiber-insertion to the fabric

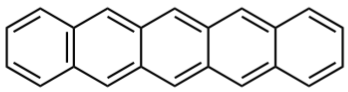


Materials



P(VDF-TrFE) copolymer

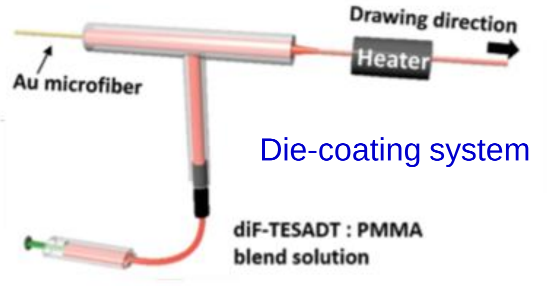
- Gate Dielectric
- Ferroelectric polymer
- Large remnant polarization
- Non-volatile memory application
- Solution processsability



Pentacene

- Organic semiconductor
- P-type
- Thermal evaporation

Coating method

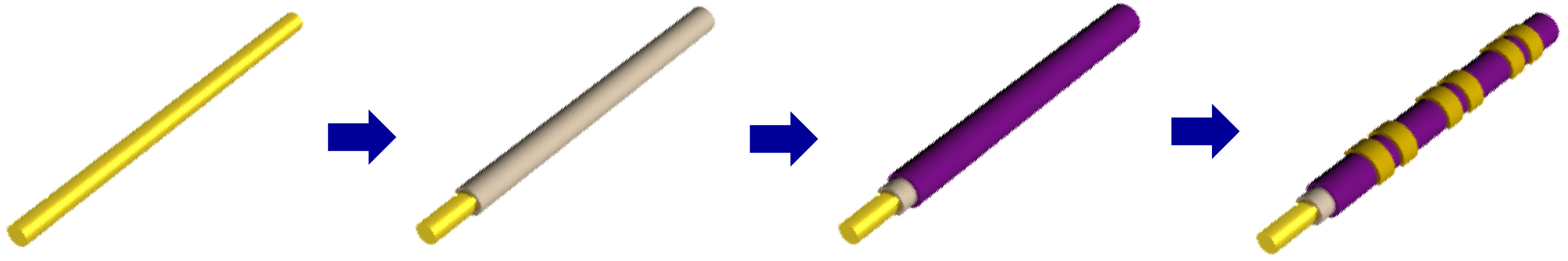


Die-coating system

Adv. Funct. Mater. 2016, *26*, 2706–2714

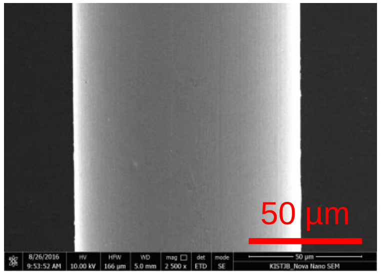
- Modified die-coating system
- Uniformly coating on the fiber

Fabrication procedure of fiber-shaped memory transistors

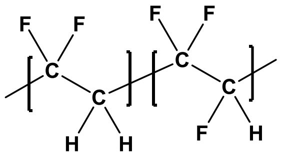


Metal wire

- Pristine gold wire
- Diameter: 100 µm

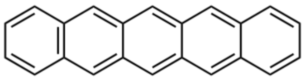


P(VDF-TrFE) coating



- 30 wt% P(VDF-TrFE) in DMF
- Capillary tube coating system
- Capillary tube(I.D.: 1.1~1.2mm)
- Coating rate: 30 mm/min
- Drying: convection oven, 140℃, 2h

Organic Semiconductor

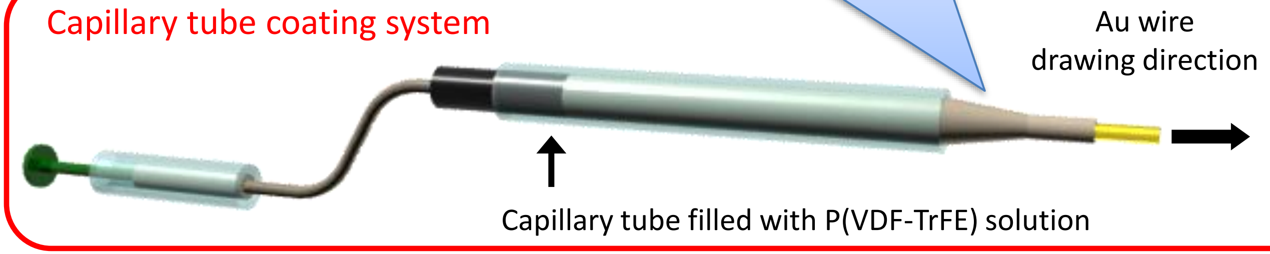


- Pentacene(50nm)
- Thermal evaporation

S/D electrode

Solution-based dielectric coating utilizing meniscus

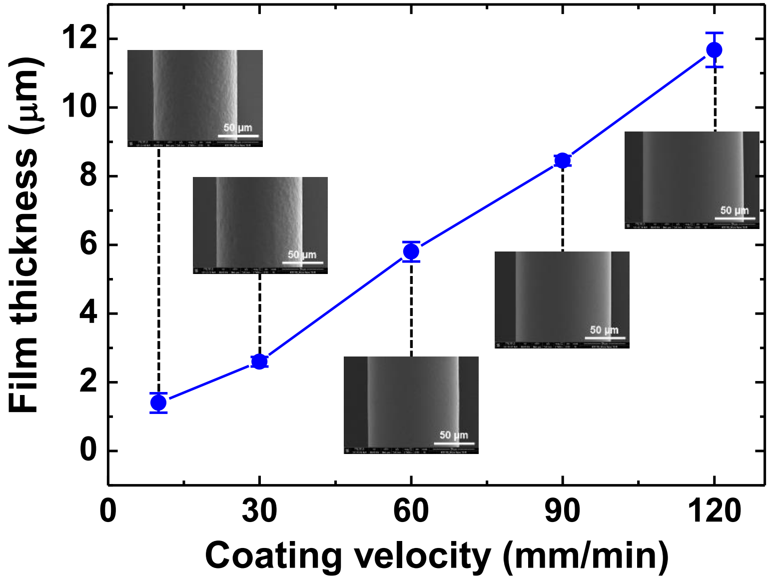
Capillary tube coating system



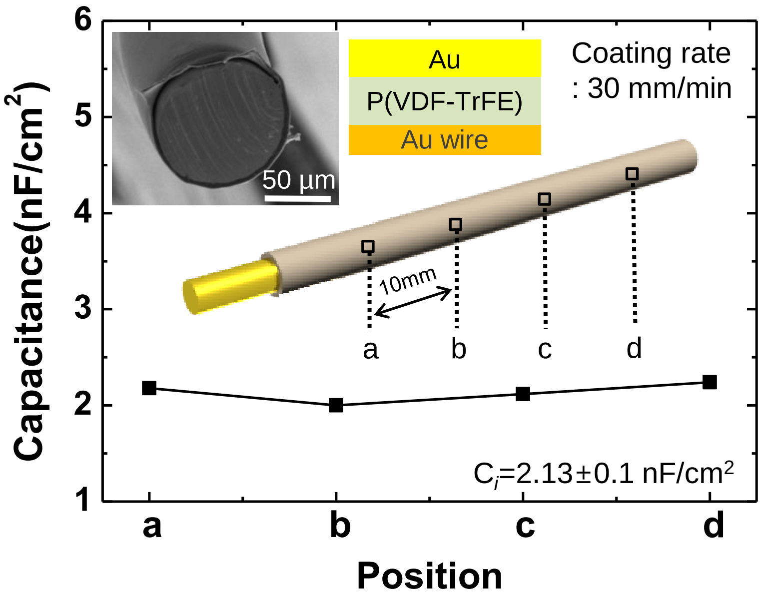
Lee et al, Manuscript in preparation (2017)

Uniformity of coated P(VDF-TrFE) film on the Au wire

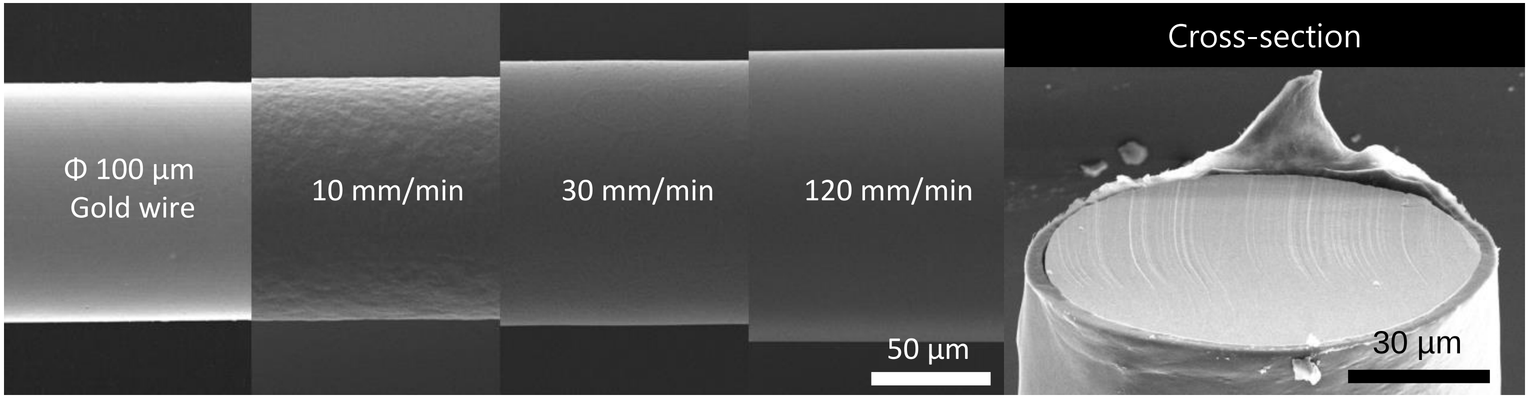
- Film thickness of P(VDF-TrFE)



- Capacitance of P(VDF-TrFE)

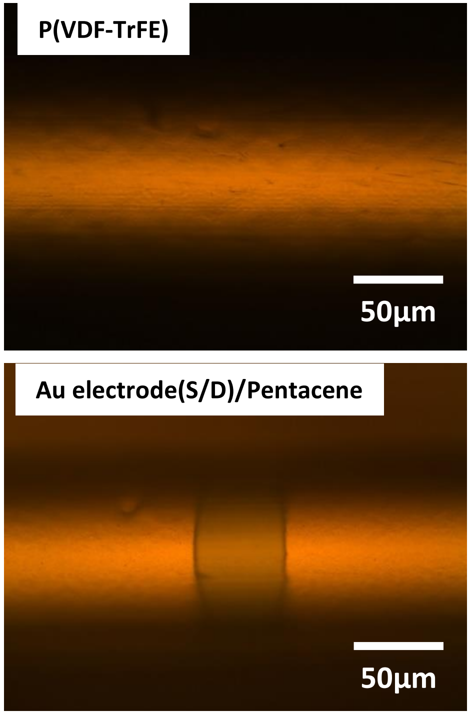


- Film thickness control depending on the coating speed

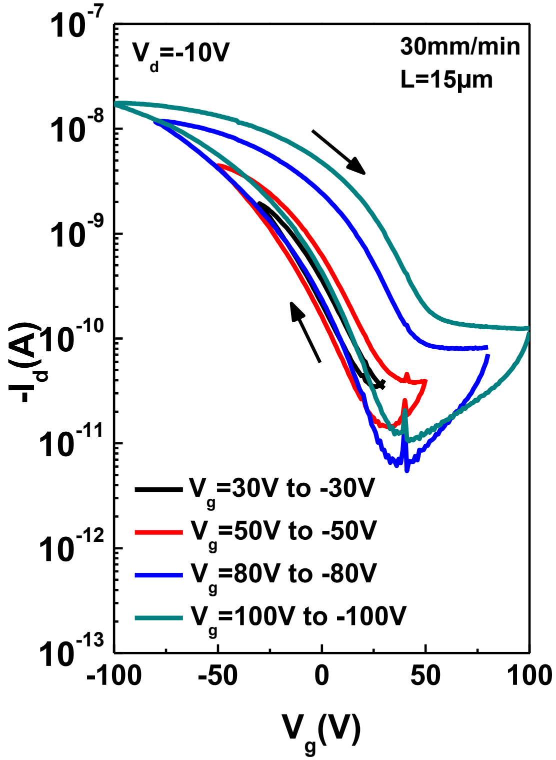


Device performances

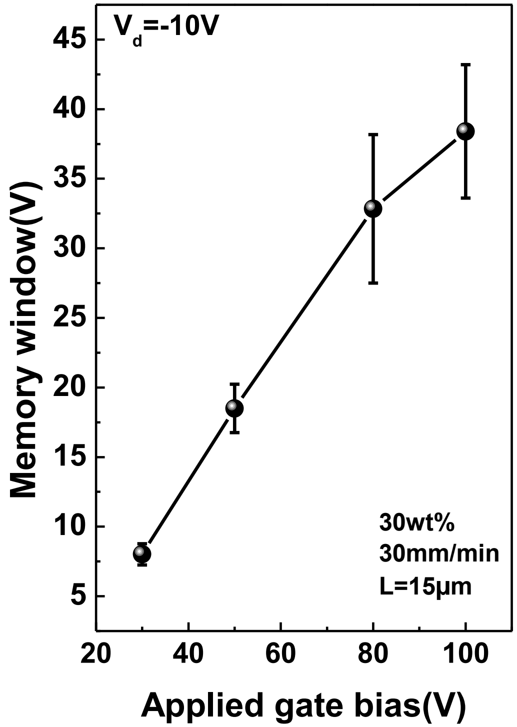
- **Optical microscope image**



- **Double sweep transfer curve**



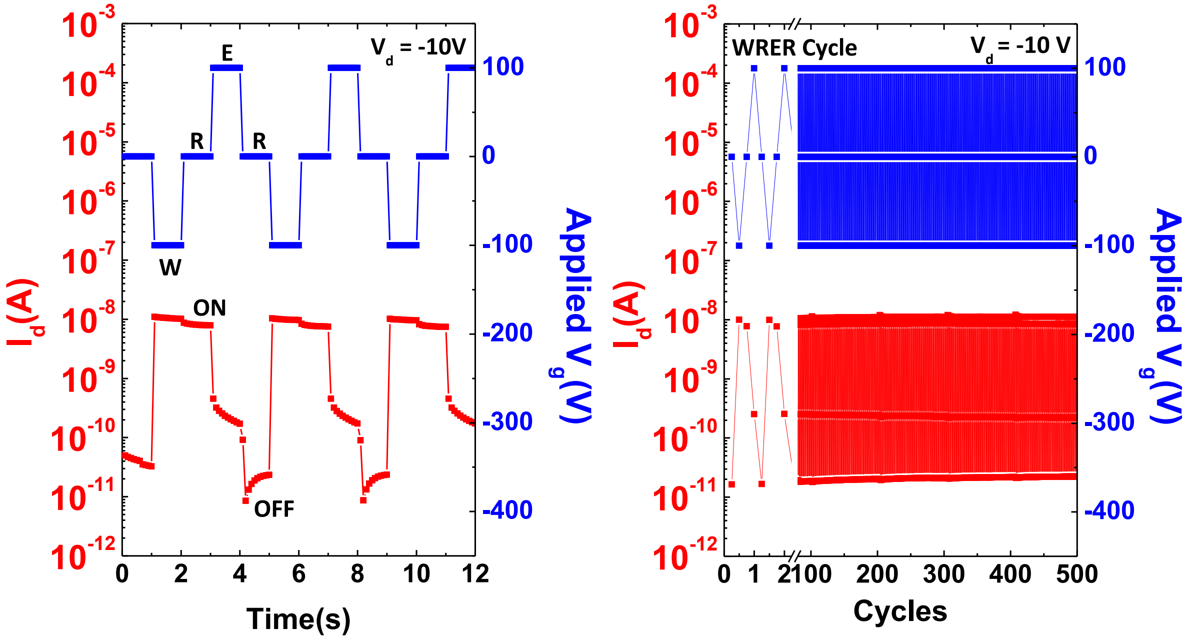
- **Memory window**



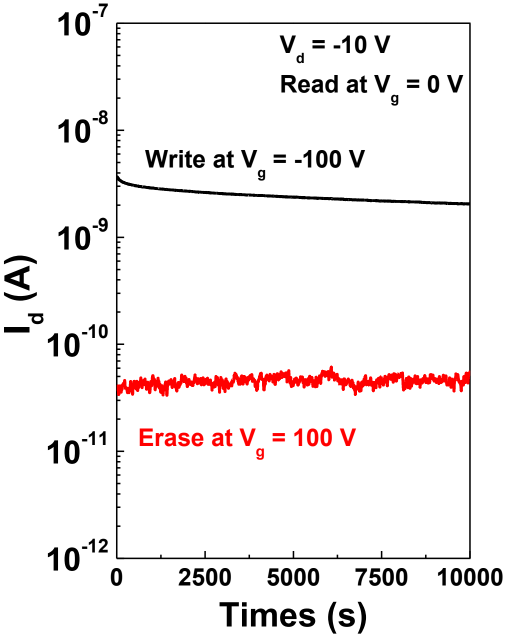
- The double sweep transfer curve showed a hysteresis loop, with a clockwise trace..
- When the gate bias sweep ranges were 30 V to -30 V, 50 V to -50 V, 80 V to -80 V, and 100 V to -100 V, the memory windows were approximately 8 V, 18 V, 33 V, and 38 V.

Device performances

- Write-Read-Erase-Read cycles



- Retention characteristics



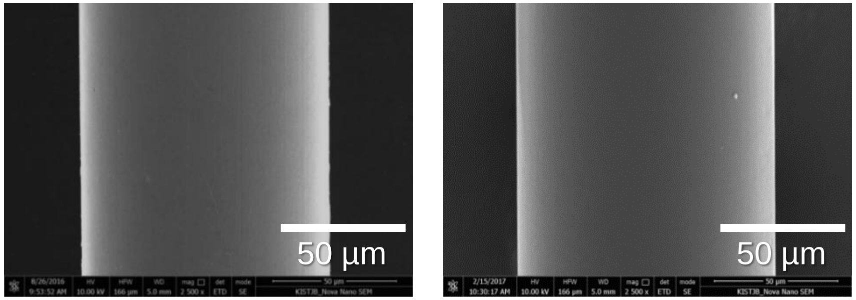
- The reversible switching properties were characterized by performing the Write/Read/Erase/Read(W-R-E-R) cycling test more than 500 times. It is worth nothing that our fiber-shaped memory transistors have reversible switching characteristics and a non-destructive readout capability.
- The measured drain current difference between ON state and OFF state was more than two orders of magnitude for 10^4 s.

Gold, Aluminum and Silver wire

- Device structure: Au/Pentacene/P(VDF-TrFE)/Metal wire(Au, Al, Ag)

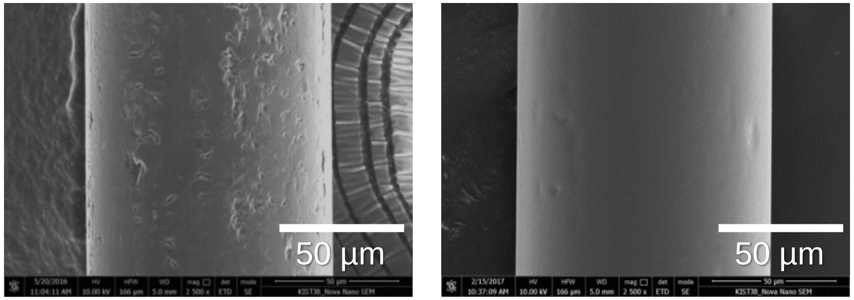
(a) Gold(Au) wire

P(VDF-TrFE): 2.6 µm



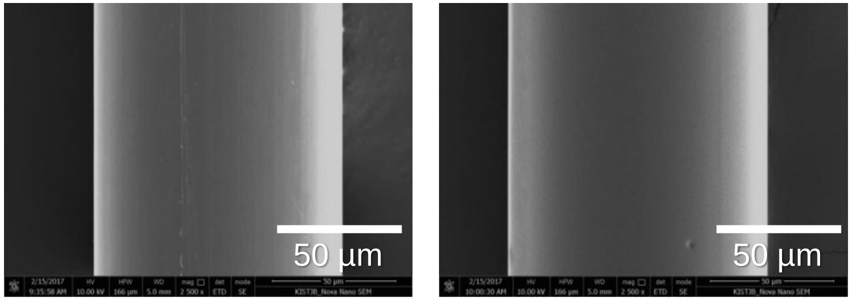
(b) Aluminum(Al) wire

1.9 µm

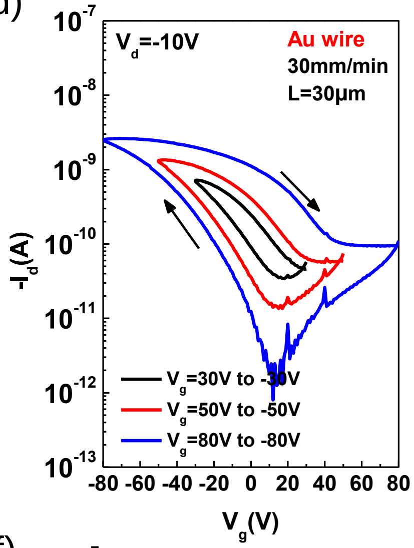


(c) Silver(Ag) wire

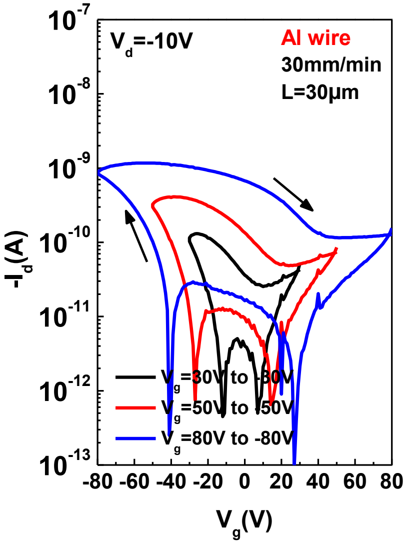
3.3 µm



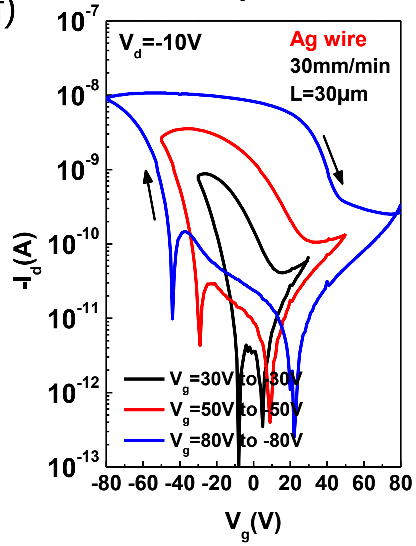
(d)



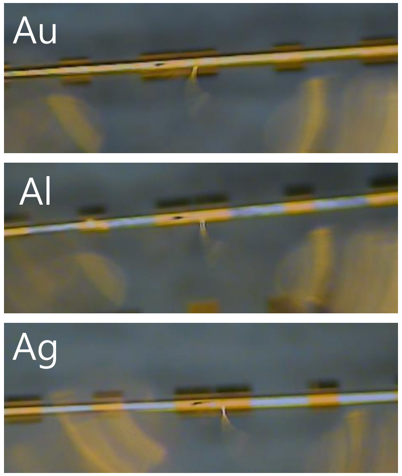
(e)



(f)



(g)

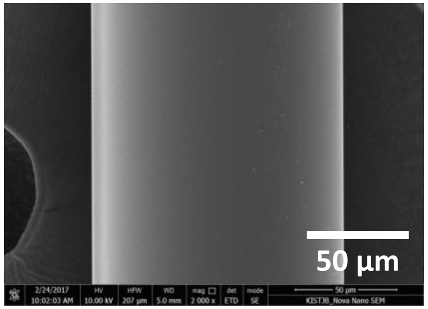


Optical fiber and Plastic fiber

- **Device structure: Au/Pentacene/P(VDF-TrFE)/Ag/Optical fiber or Plastic fiber**

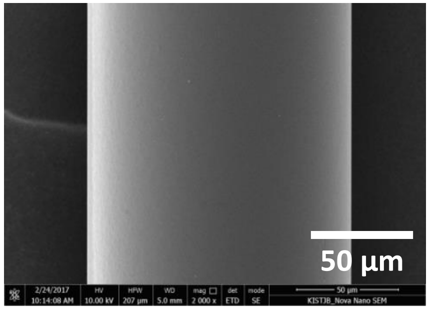
➢ SEM images

(a) Optical fiber(OptF)



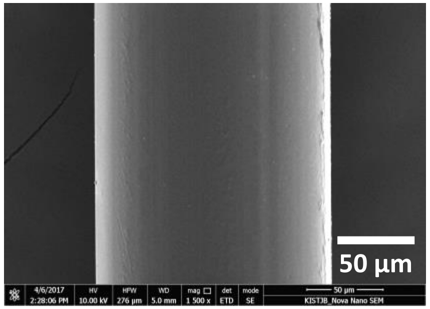
Diameter: 125 µm

(b) P(VDF-TrFE)/Ag/OptF



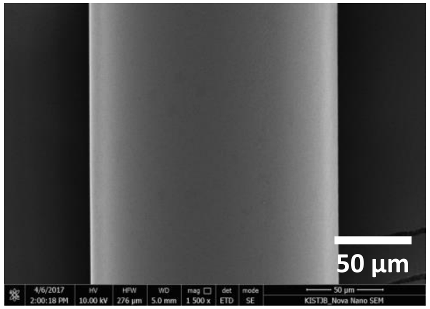
P(VDF-TrFE): 2.9 µm

(c) Plastic fiber(PF)



Diameter: 155 µm

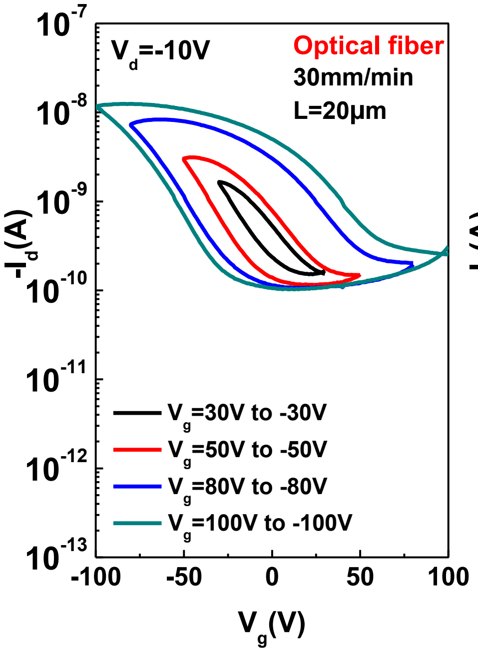
(d) P(VDF-TrFE)/Ag/PF



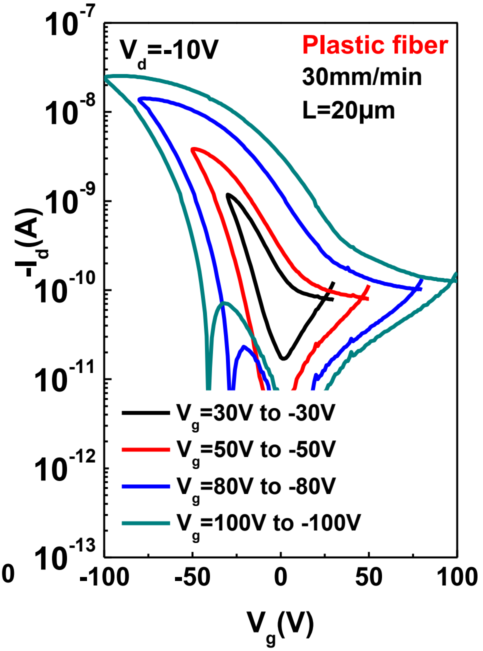
P(VDF-TrFE): 3.7 µm

➢ Transfer characteristics

Optical fiber



Plastic fiber

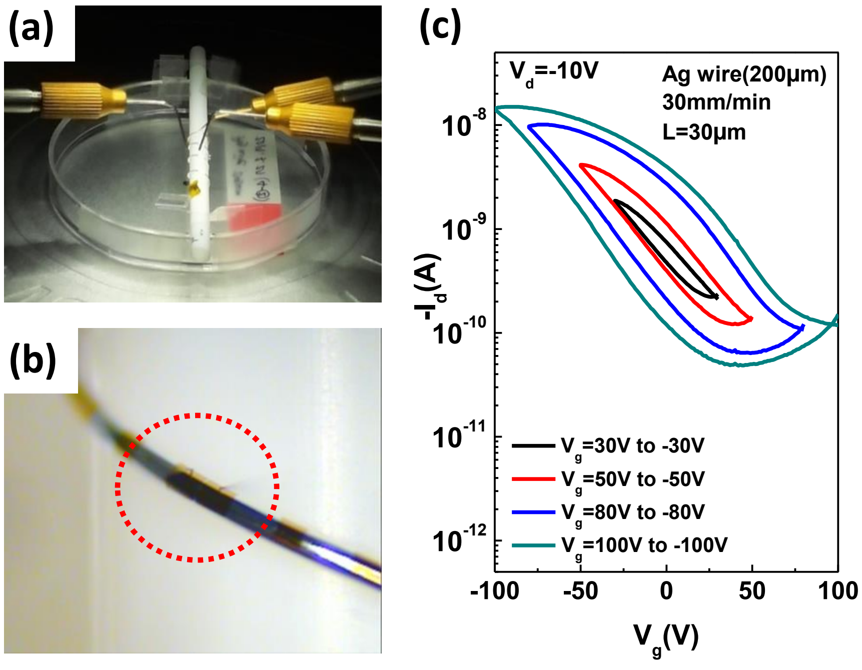


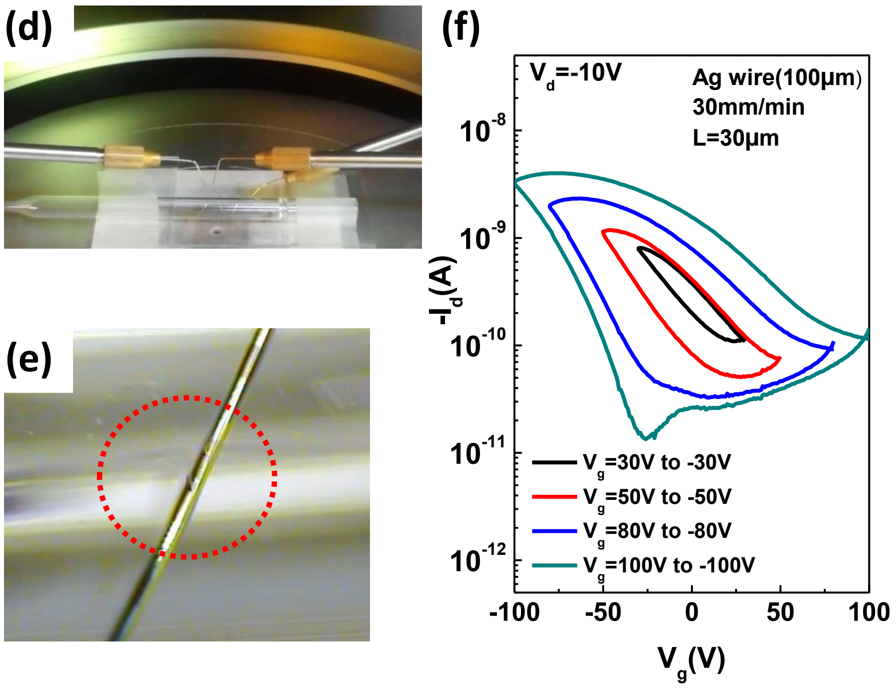
Optical fiber and Plastic fiber

- Device structure: Au/Pentacene/P(VDF-TrFE)/Ag wire

➢ Winding on straw
  - Diameter of Ag wire: 200 µm
  - Diameter of straw: 3.6 mm

➢ Winding on **glass pipette**
  - Diameter of Ag wire: 100 µm
  - Diameter of glass pipette: 7.1 mm

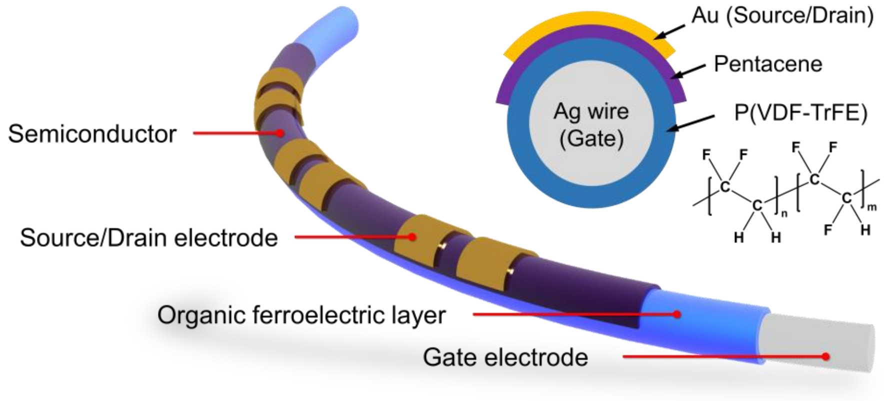


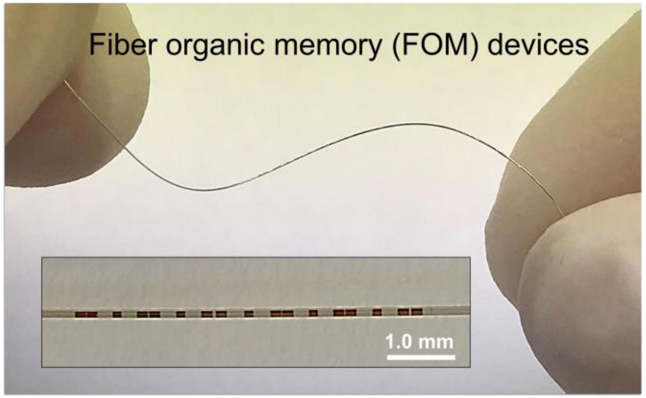


Lee et al, Manuscript in preparation (2017)

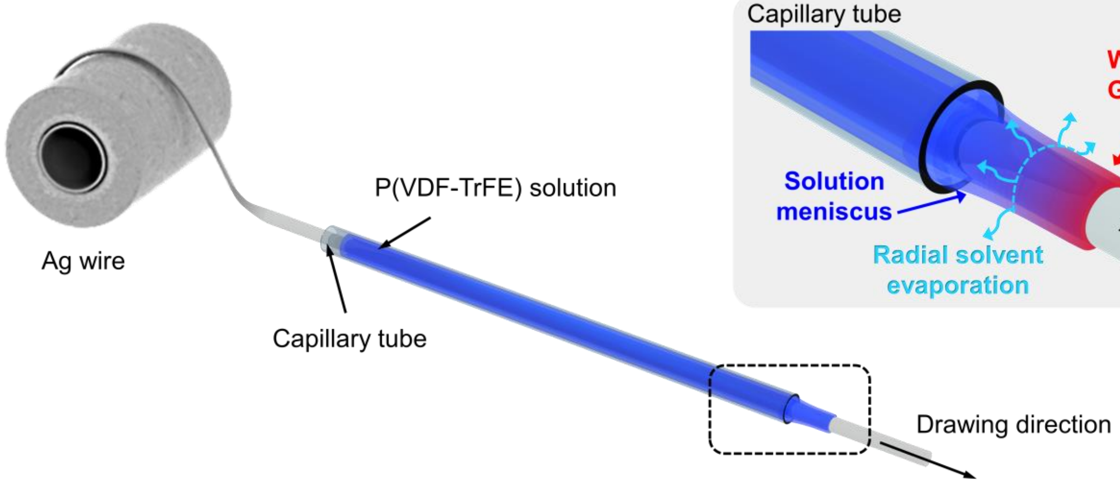
Low-Voltage Fiber memory Transistor

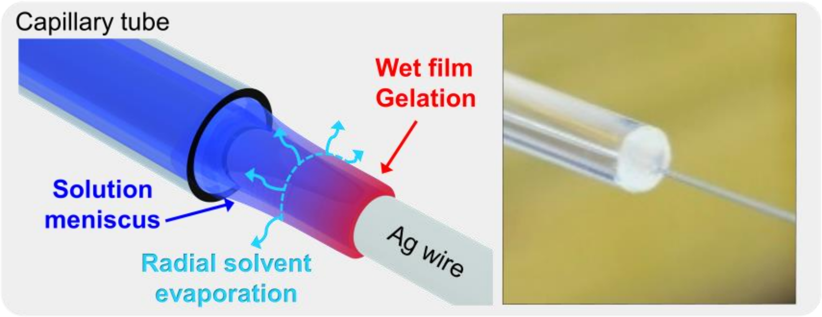
- Optimization of Coating process



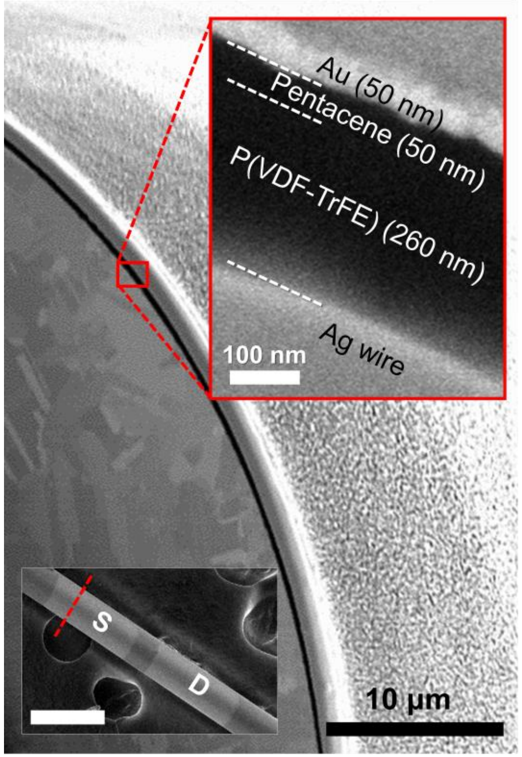


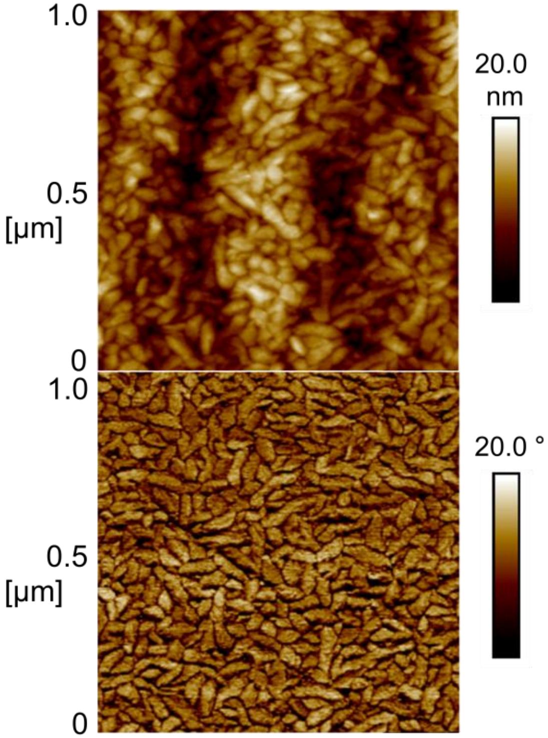
Capillary Tube-Assisted Coating (CTAC) Prcess

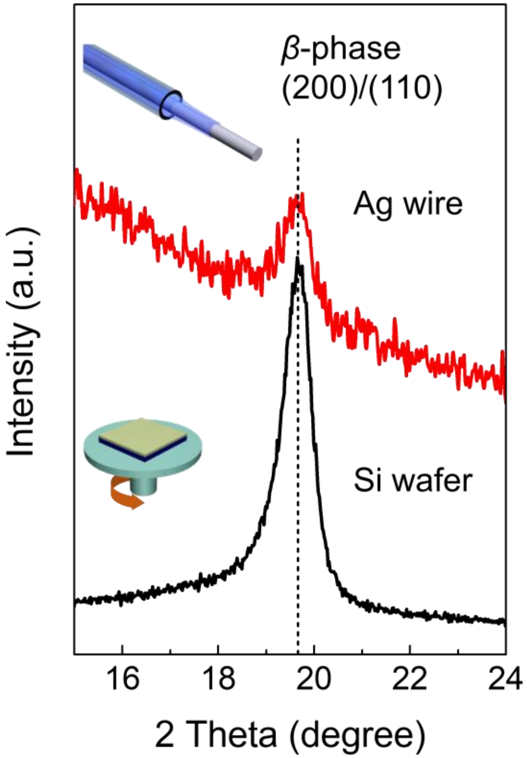




Low-Voltage Fiber memory Transistor

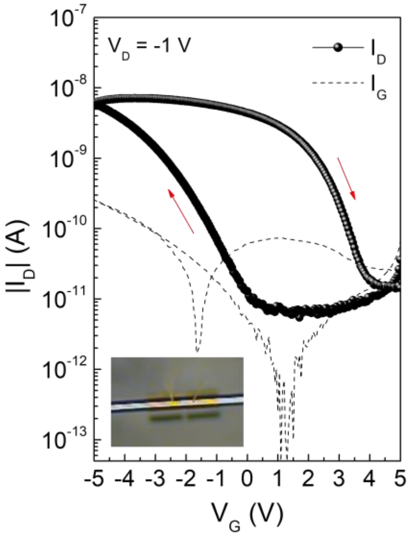


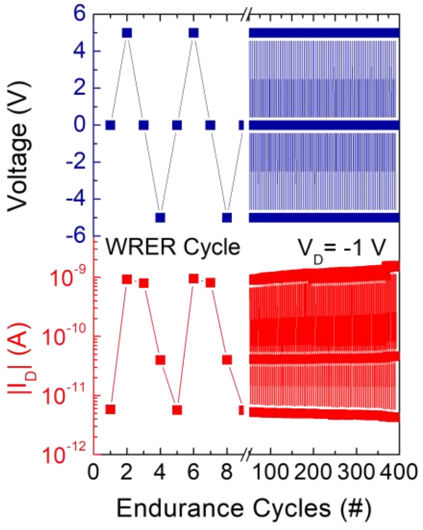


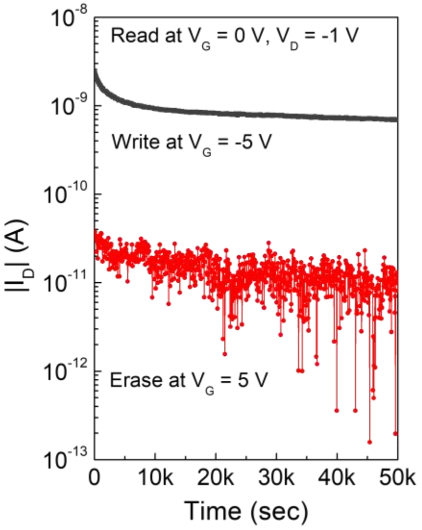


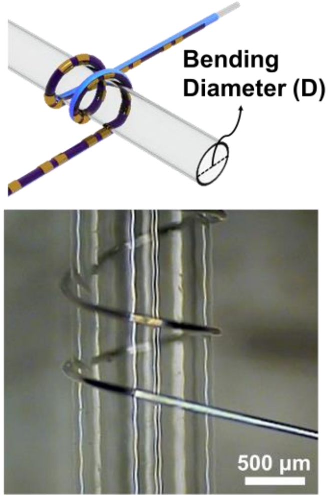
Low-Voltage Fiber memory Transistor

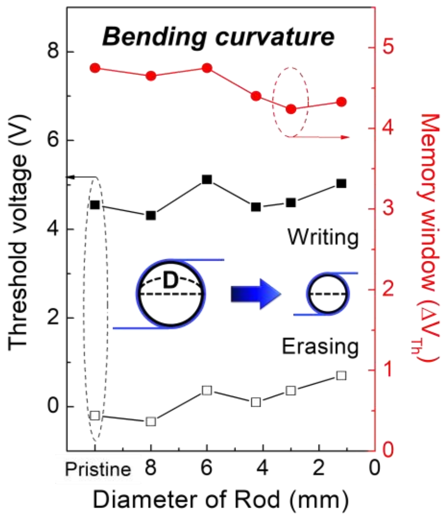
- Device Performances

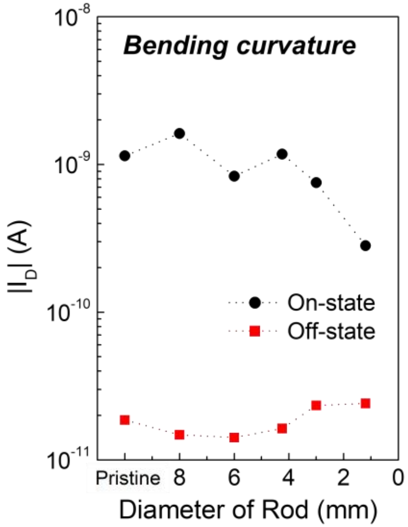










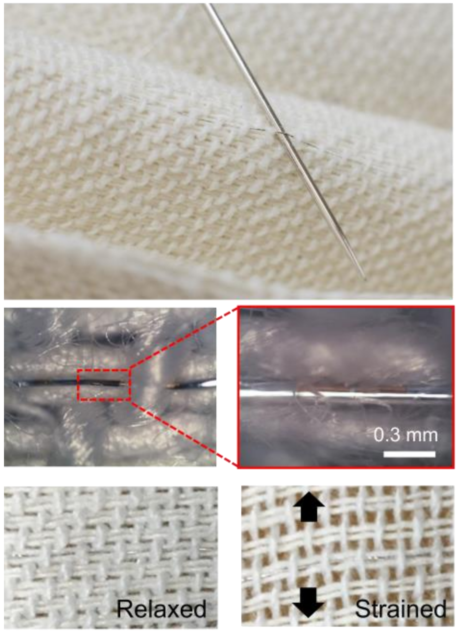


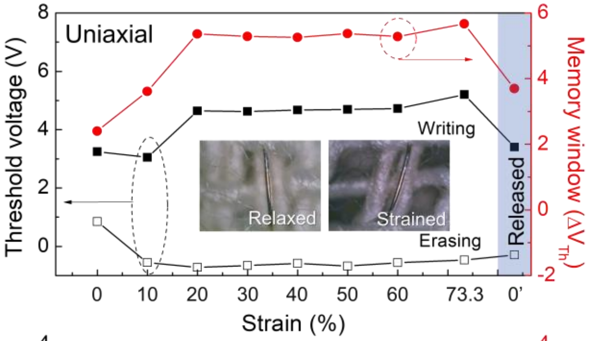
Low-Voltage Fiber memory Transistor

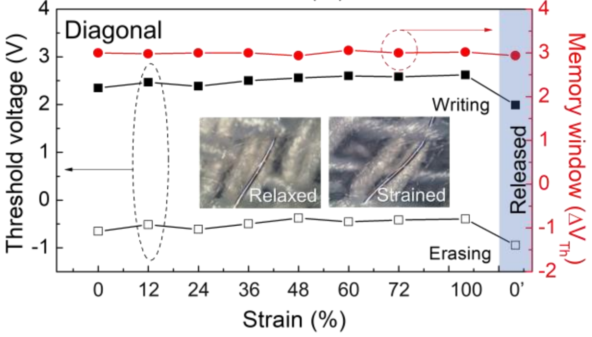
- Fiber memory in a textile

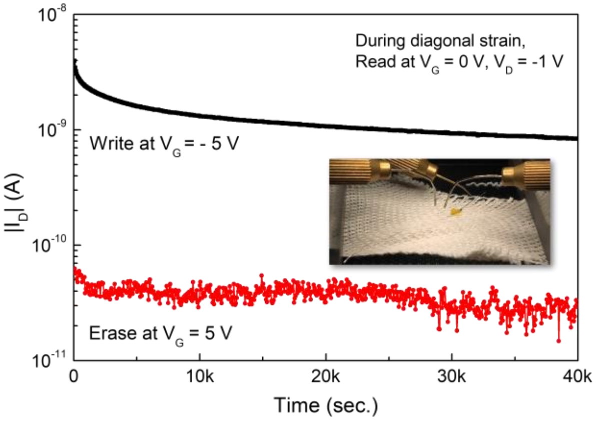
Low-Voltage Fiber memory Transistor

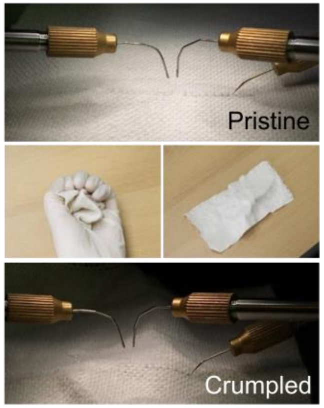
- Performance of Fiber memory in a textile

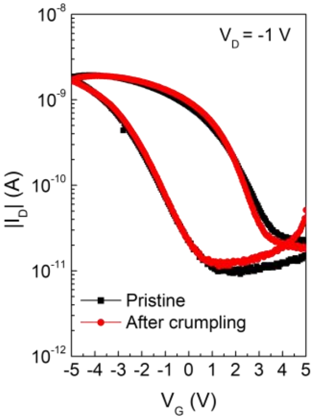






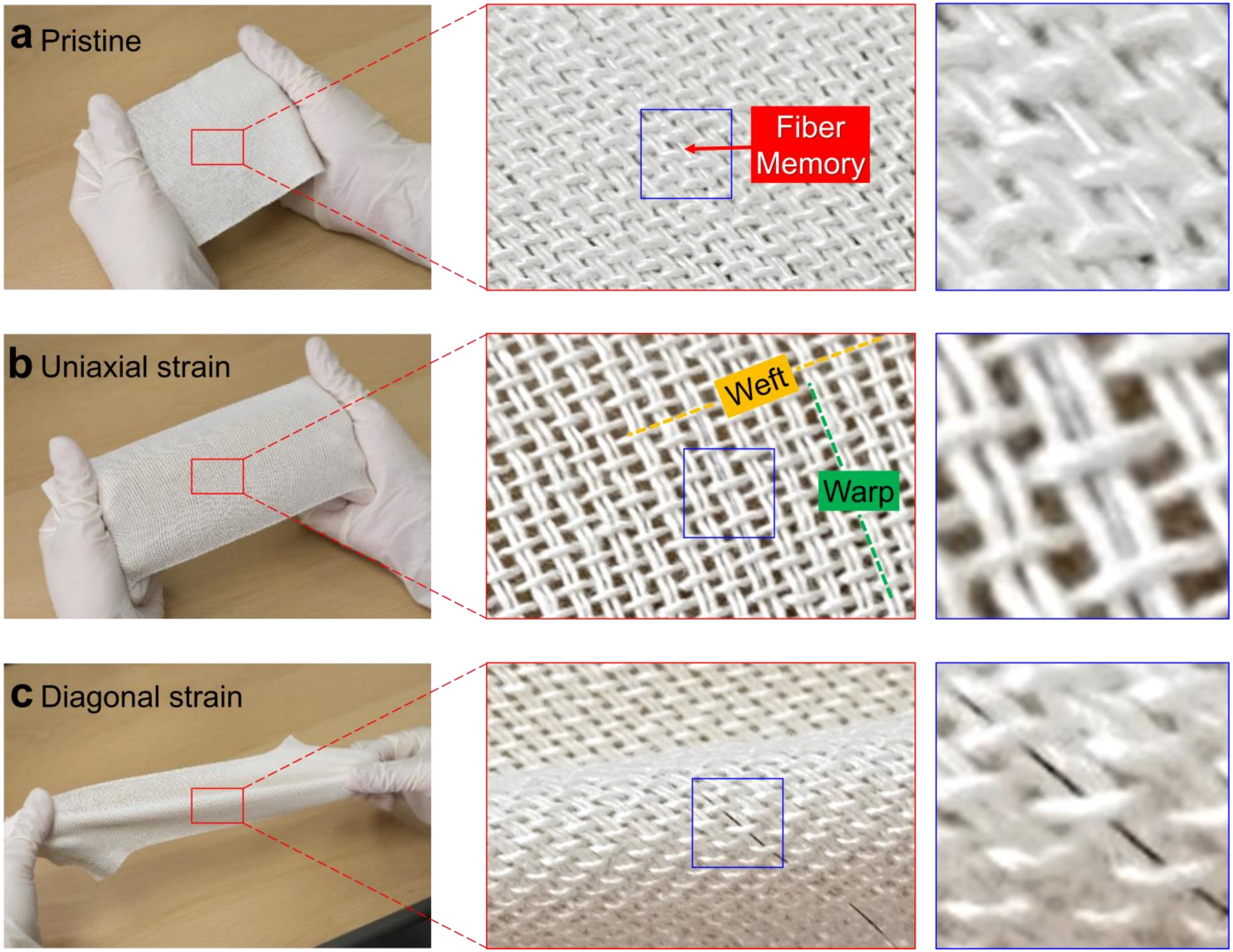






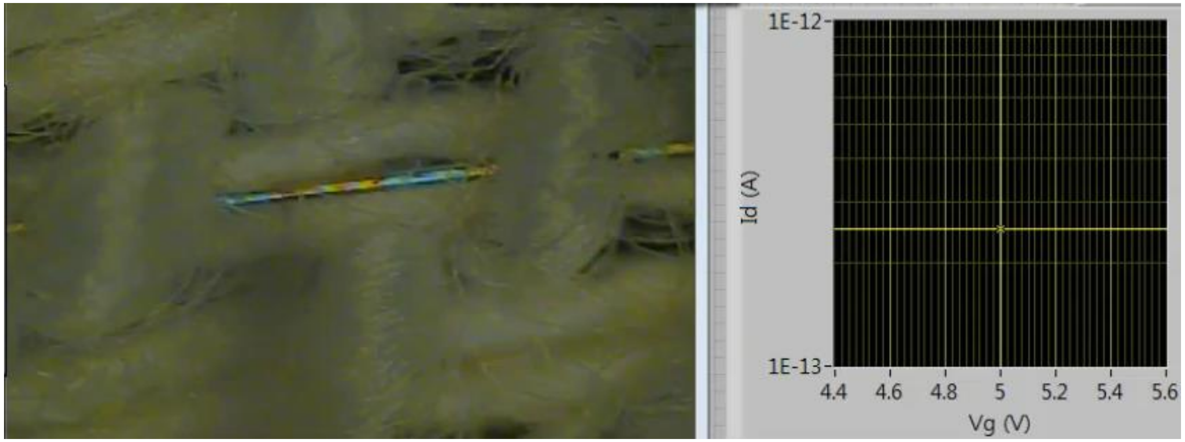
Low-Voltage Fiber memory Transistor

- Fiber memory in a textile under various strain conditions

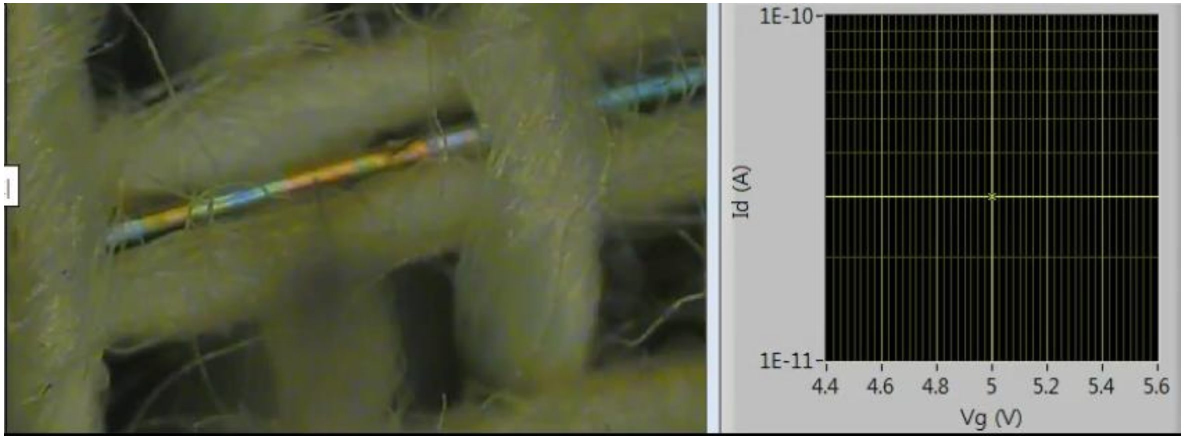


Low-Voltage Fiber memory Transistor

- Pristine



- 73.3 % strain



Next-generation Wearable Device Platform

Chip on a Fiber for New concept of E-Textile

Future of Wearable Computer ?

Wearable Devices for Future Emerging Technology

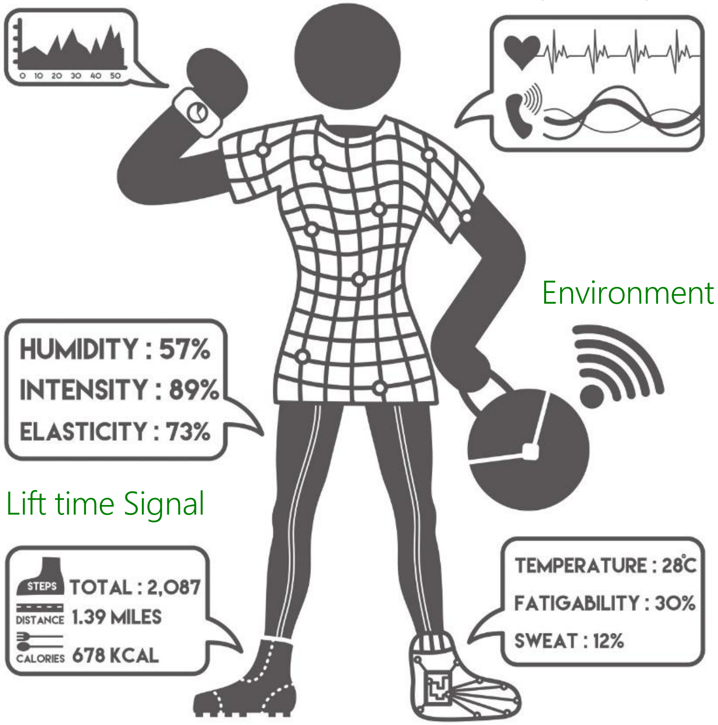
Requirements for Wearable Devices

- Main concept of Wearable Devices

Organic Signal

Environment Signal

Lift time Signal



From: Designgounge

- Functions (Performance)

유의미한 데이터의
수집 (Sensing)
처리 (Processing)
저장 (Memory)
표시 (Displaying)
전송 (Data transmission)

- Shape (Platform)

Interactive Device Technology

; The technology includes processing, sensing, displaying, memory, and transfer of the signals from human body environment

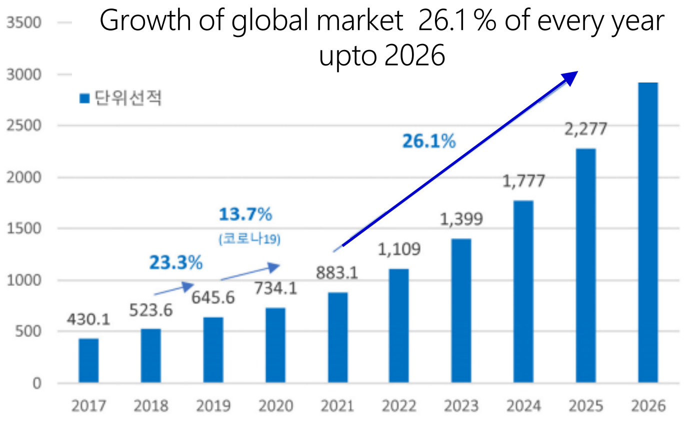
Perspectives on Wearable Devices

Expectation on the technology and market

Growing up glove market

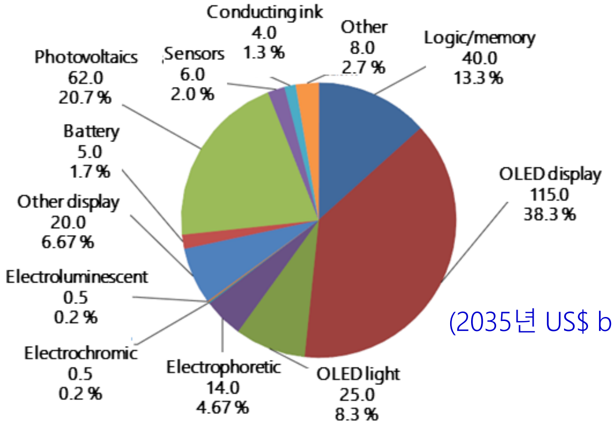
From: Credit Suisse(2013.5) The Next Big Thing-Wearable Are In Fashion

Perspectives on Global market



Frorm: Frost & Sullivan (2021)

Global market share of wearable technlology



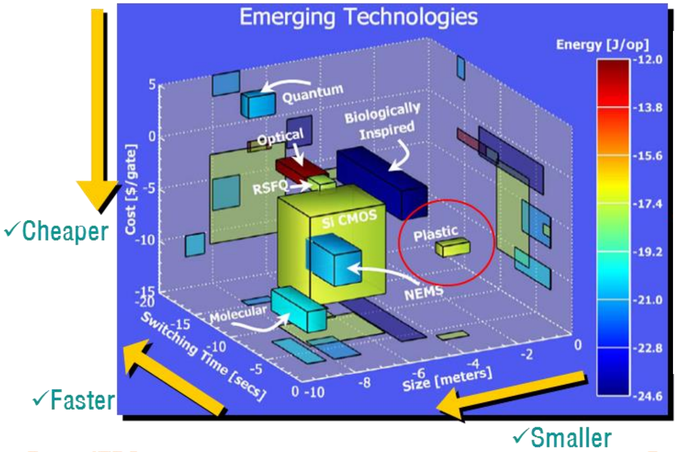
(2035년 US$ billion)

From: IDTechEx 2015-2025

Research Trend on Wearable Devices

Research

Issues on emerging electronic devices



Keywords
- Low cost
- Heat
- Synthesis
- Flexibility
- Printing
- Robustness
- Reliability
- Scaling down
- Uniformity

●From ITRS (International Technology Roadmap for Semiconductors) Roadmap Emerging Technologies*

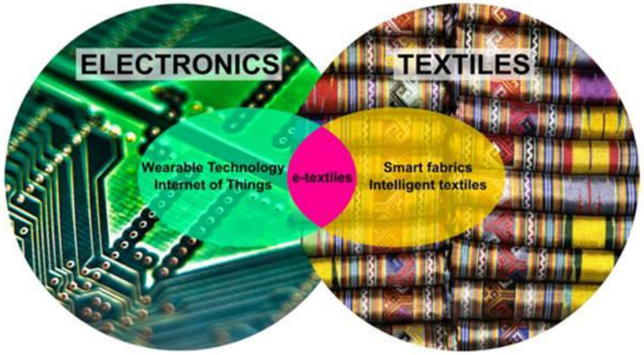
Requirements on Future Devices

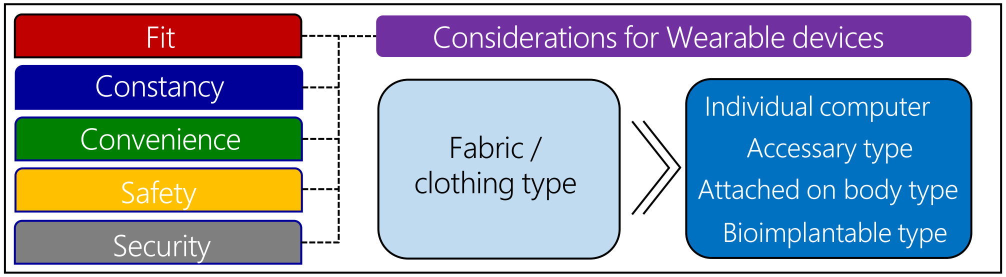
Current Requirement [Speed, Size] Capacity

Feeling, Convenience, Wear] New Requirement

Electronic Devices with various Functions and their shape

Electronic Textile: Implementation of Electronics on Fabrics or Fiber (non conventional substrate)





- Fit
- Constancy
- Convenience
- Safety
- Security

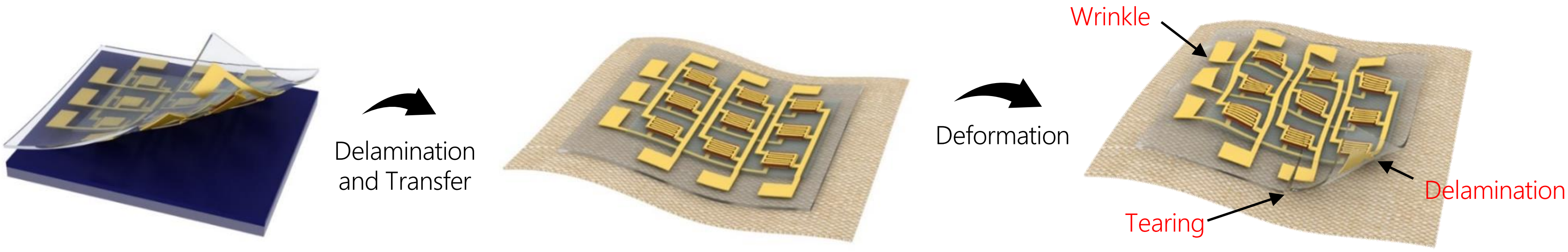
Considerations for Wearable devices

Fabric / clothing type 〉 Individual computer, Accessary type, Attached on body type, Bioimplantable type

Limitation of Conventional Electronic Textile

What is the best platform for wearable electronics?

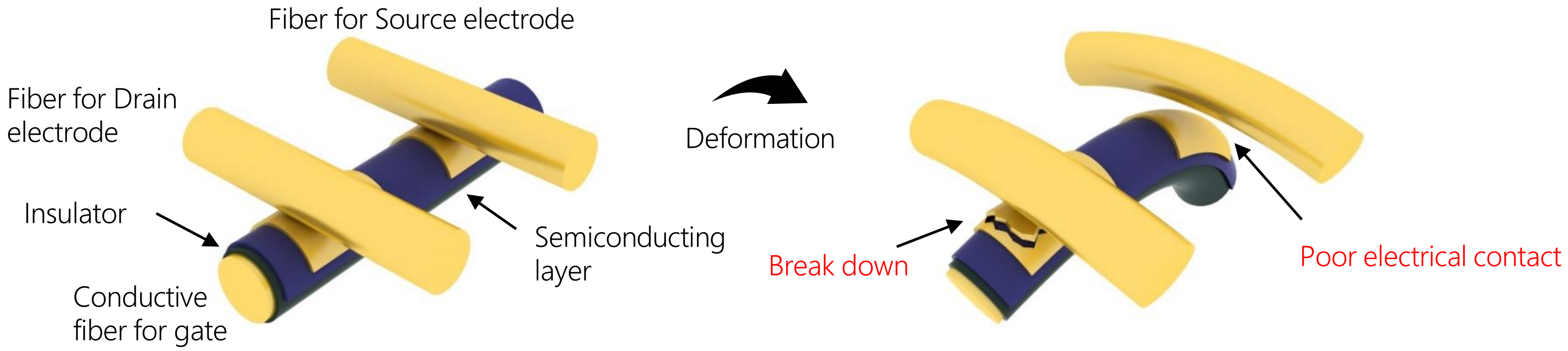
- Flexible electronic device on flat substrate



Fabricated on rigid Sub.

Flexible devise right after transfer on Fabrics

- Electronic fiber by weaving technology



- Limitations in Scaling down, High performance, Robustness on device operation

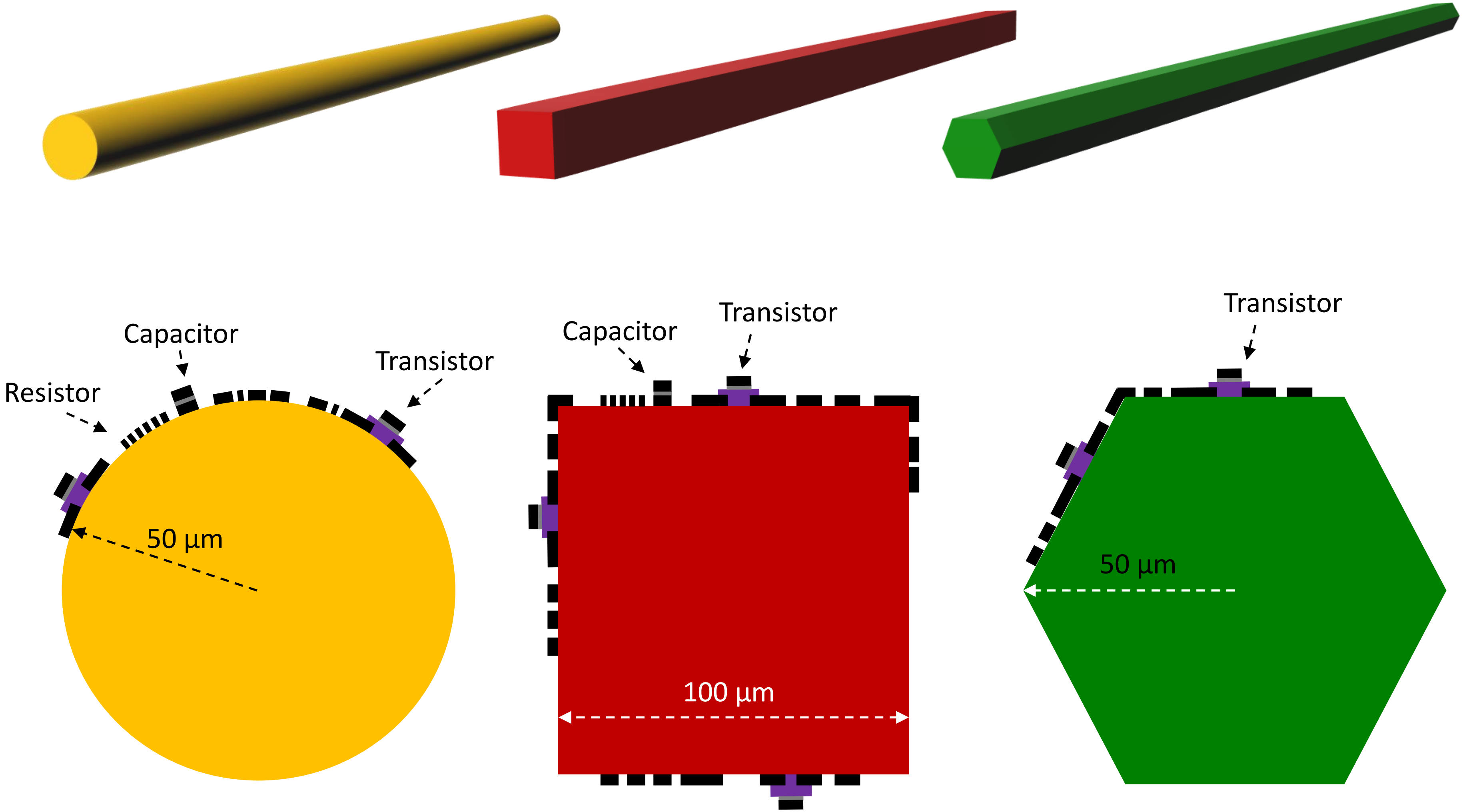
▶ Required innovative Platform for wearable electronics

Chip on a Fiber

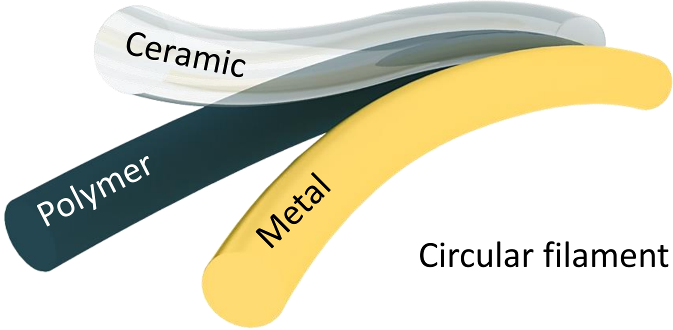
Circular

Rectangular

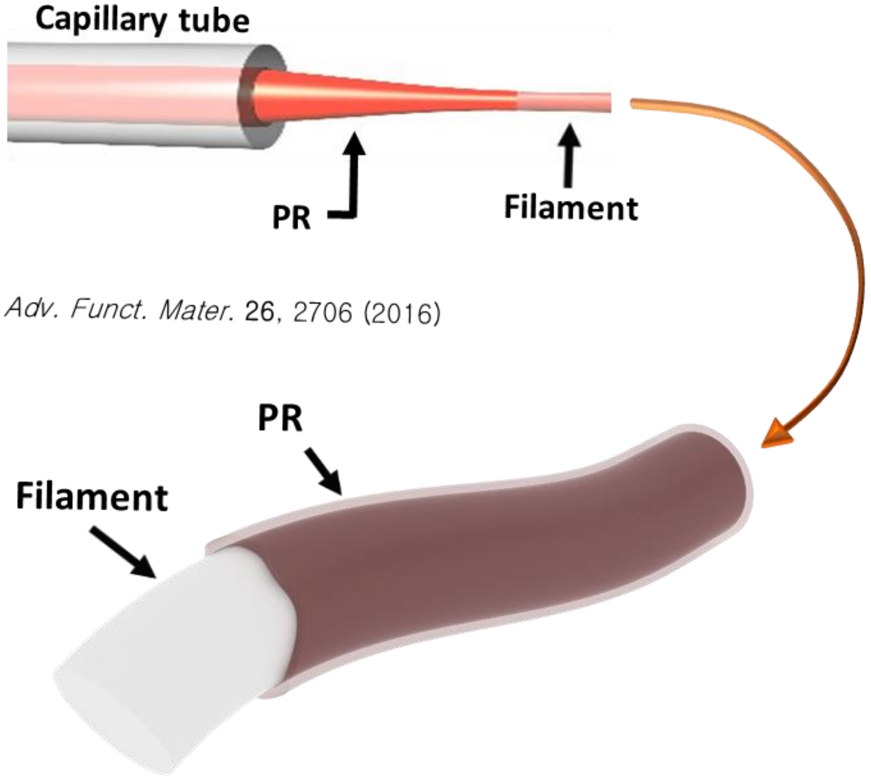
Polygonal



Coating process for Chip on a fiber



PR coating process on filament



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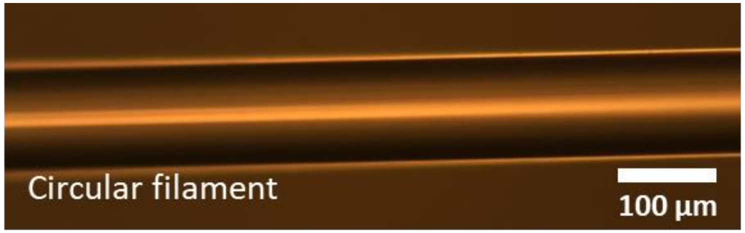
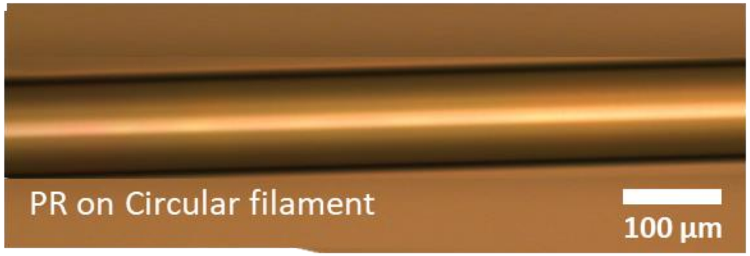
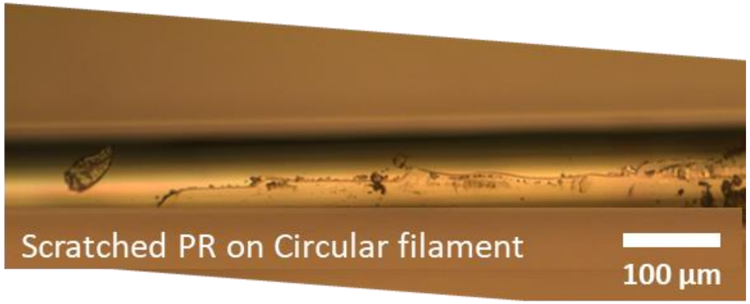
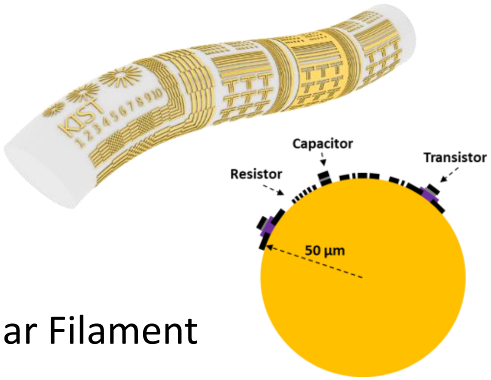




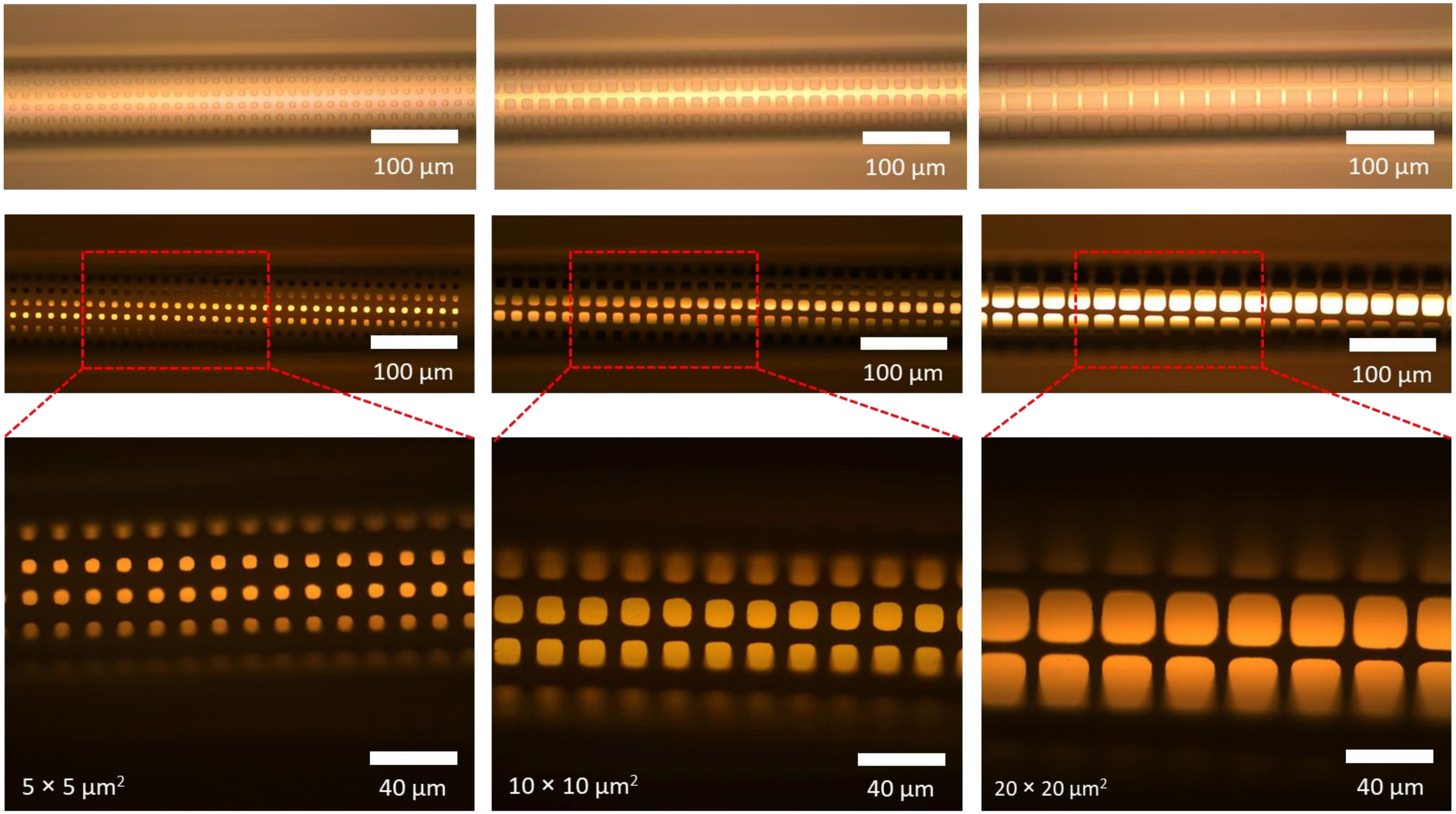


Chip on a fiber

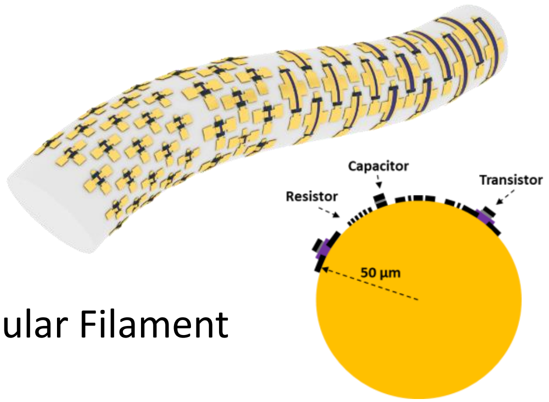


Circular Filament

Metal pattern array on fiber

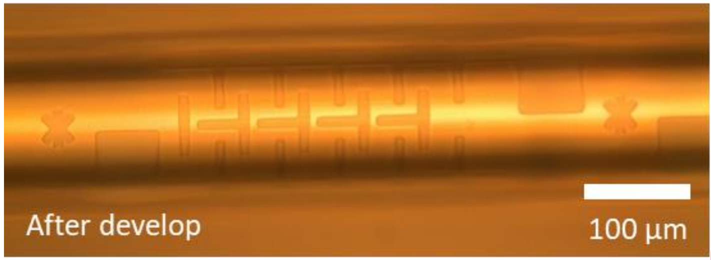


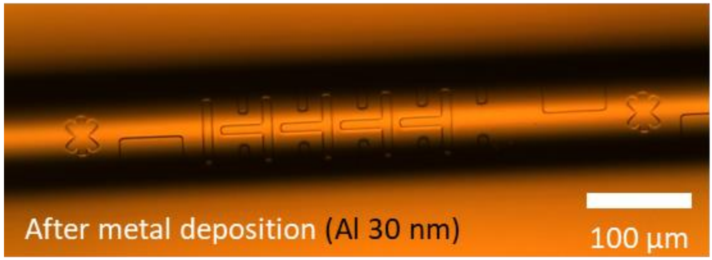
Chip on a fiber

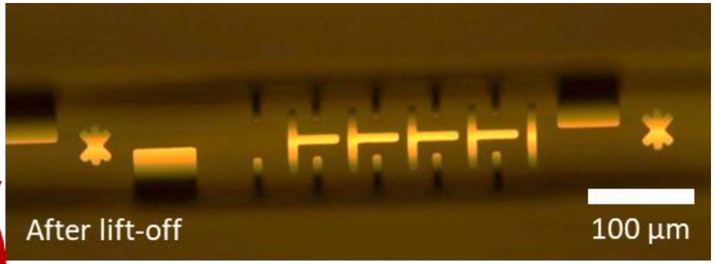


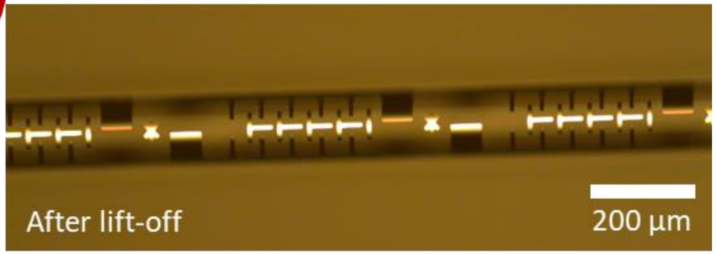
Circular Filament

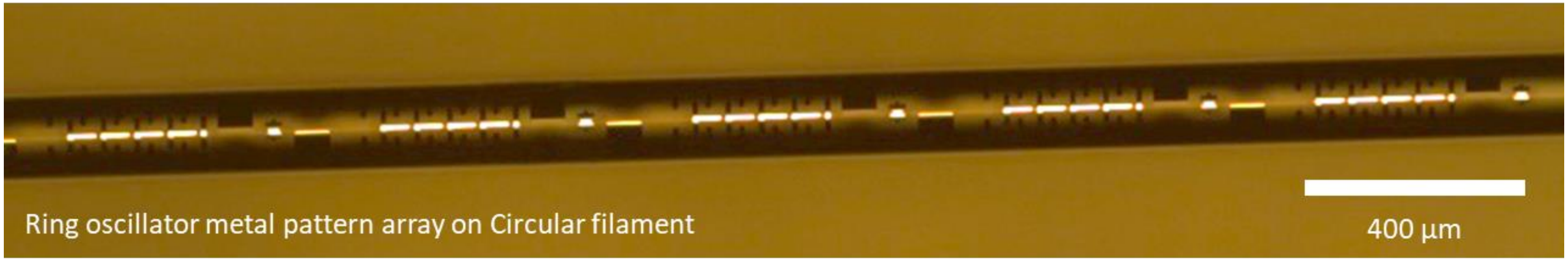
Circuit electrode on fiber


After develop

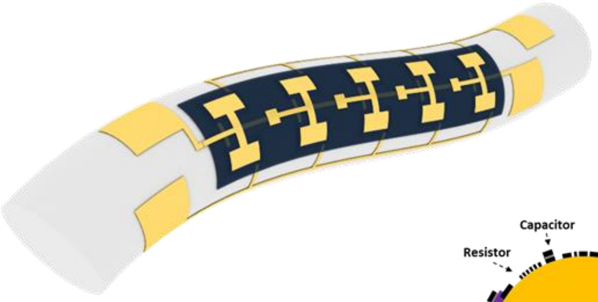

After metal deposition (Al 30 nm)


After lift-off

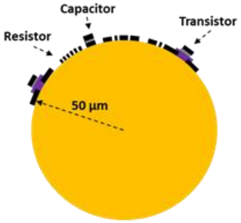

After lift-off

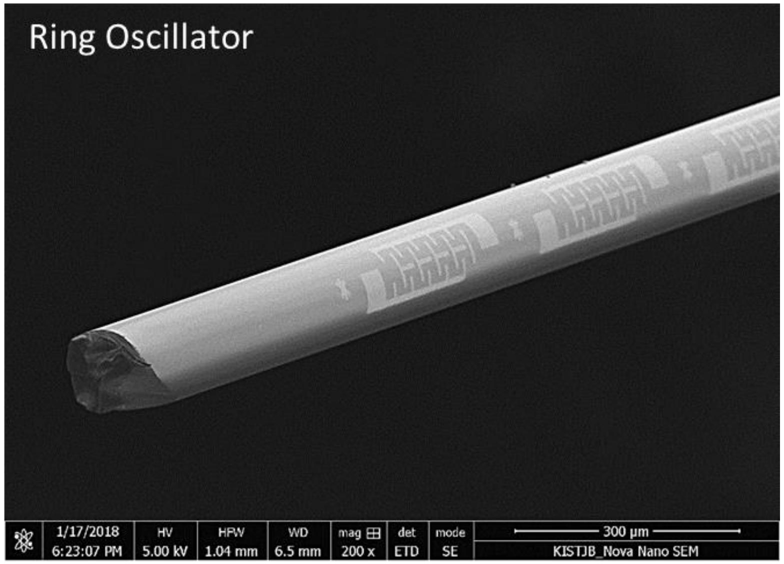

Ring oscillator metal pattern array on Circular filament

Chip on a Fiber

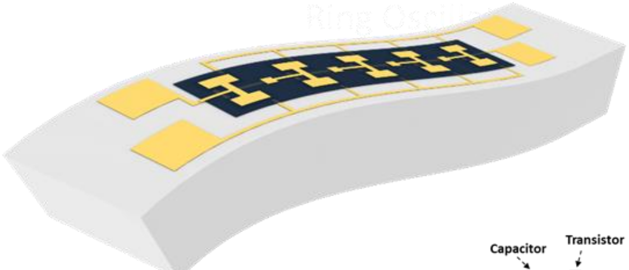


Circular Filament

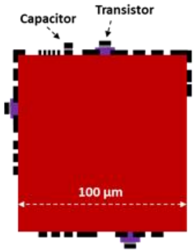


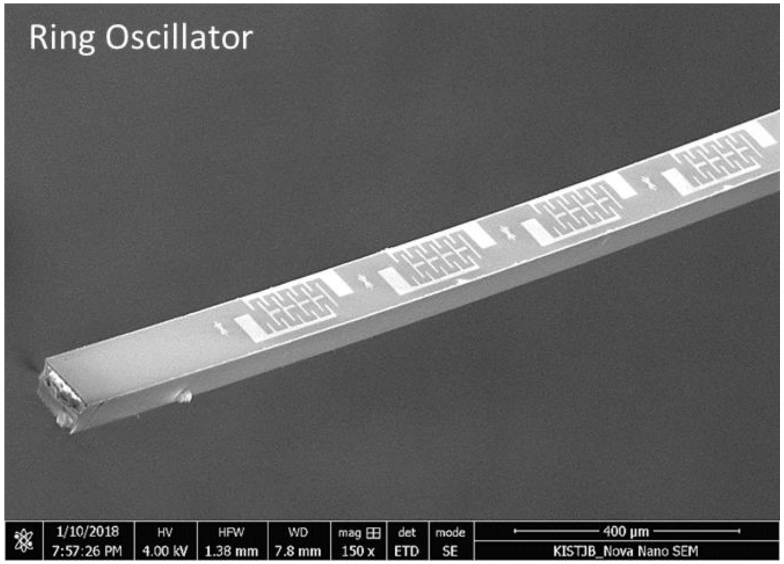


Ring Oscillator



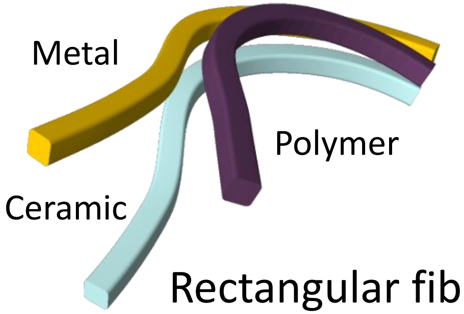
Rectangular Filament





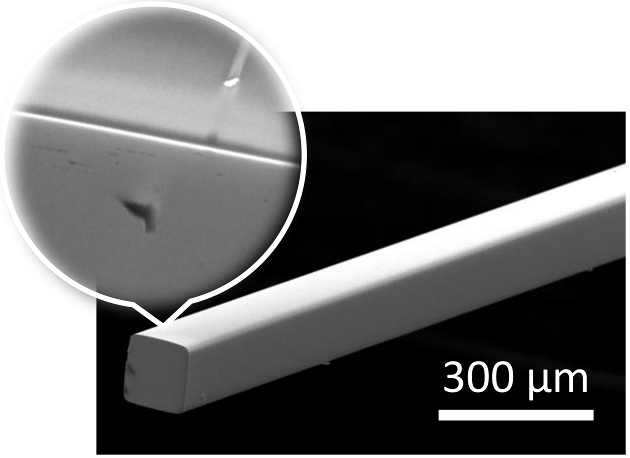
Ring Oscillator

Chip on a Fiber

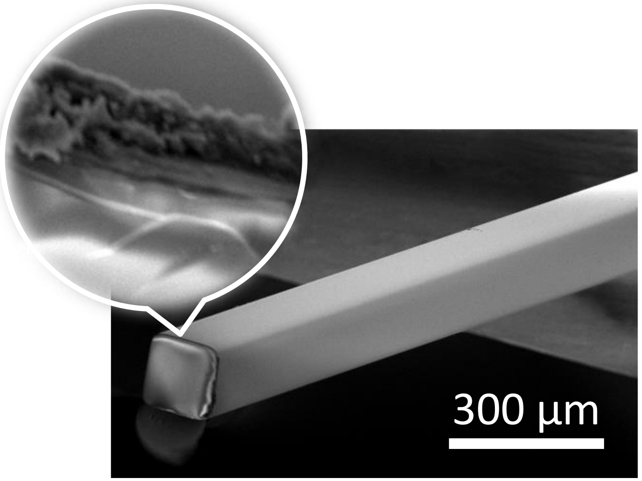


Rectangular fiber

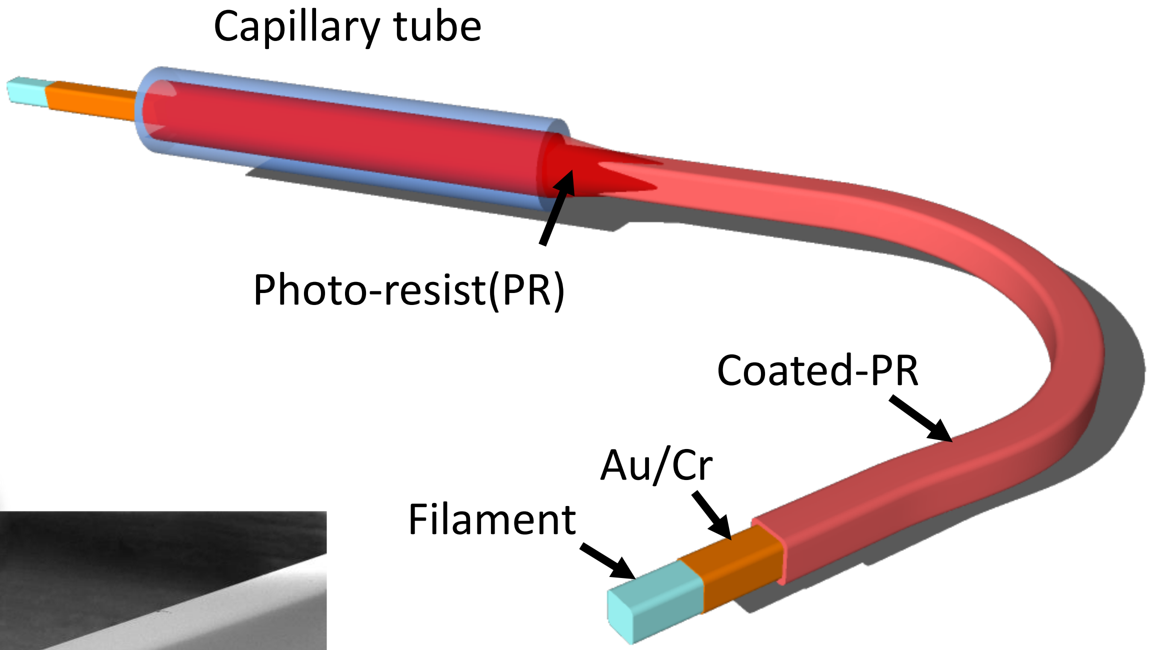
Photo-resist coating process on fiber



Metal on filament



PR on metal/filament



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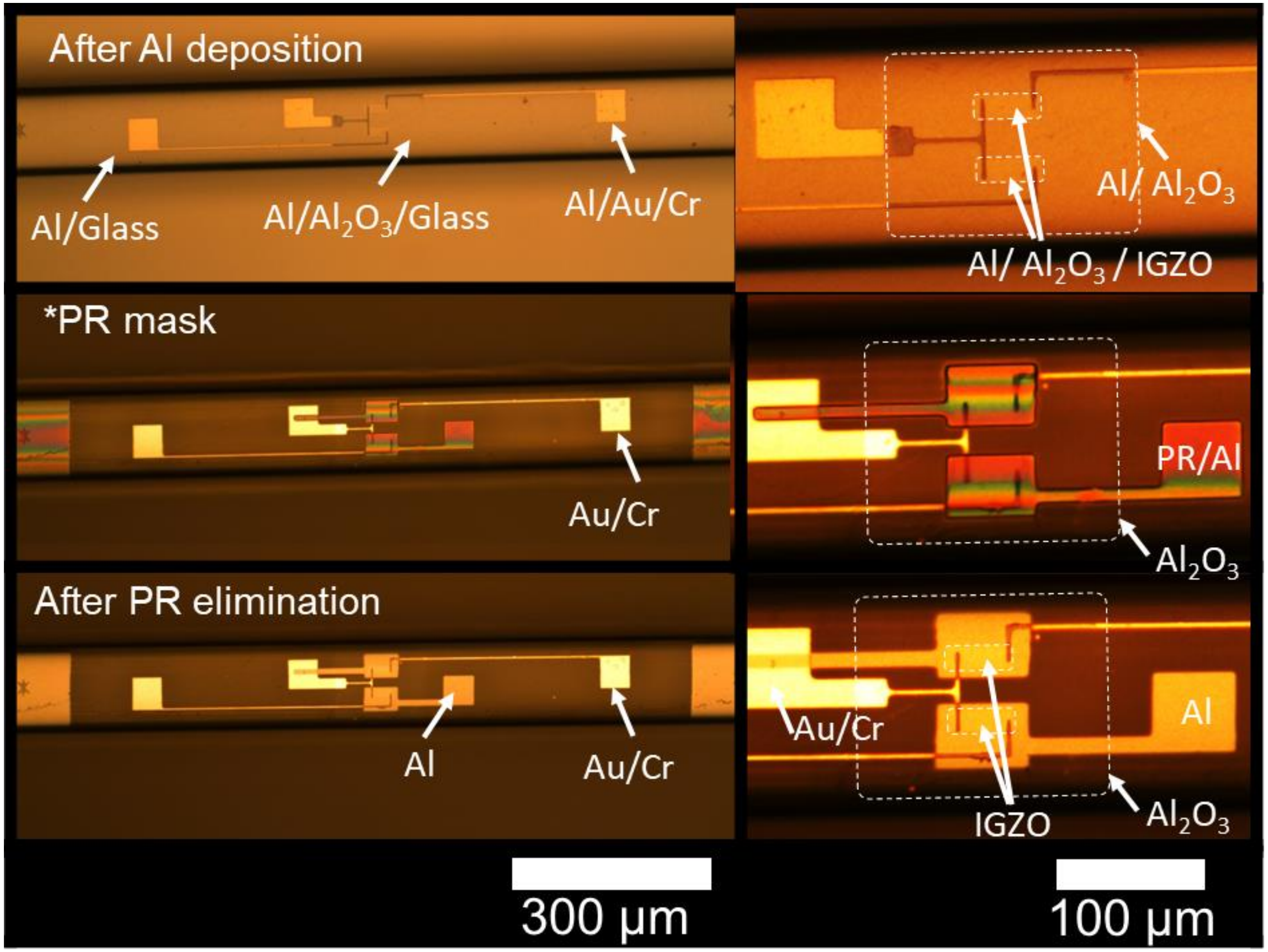
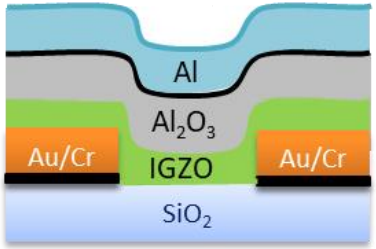
*□ 150 µm x 150 µm x 7.5 cm glass filament

Chip on a fiber

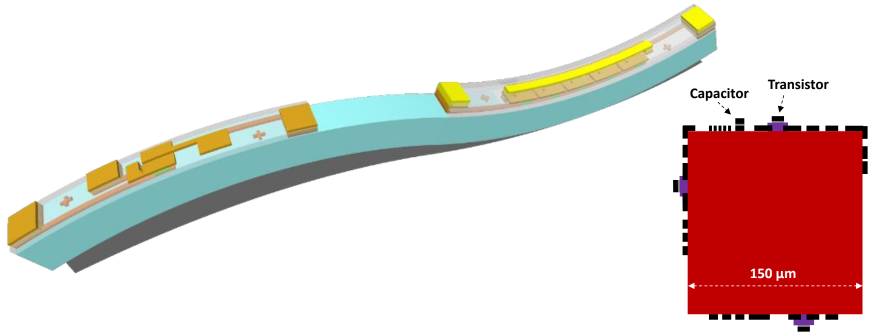
150 µm x 150 µm monofilament type device fabrication



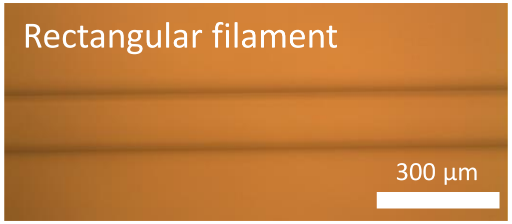


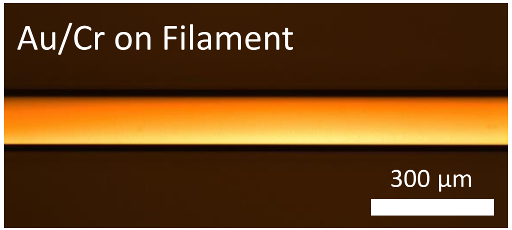
Chip on a fiber

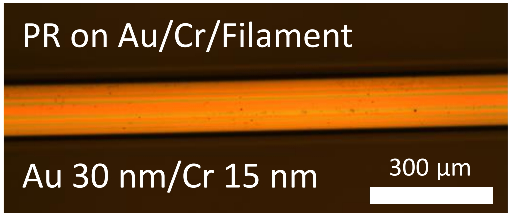
Circuit electrode on fiber



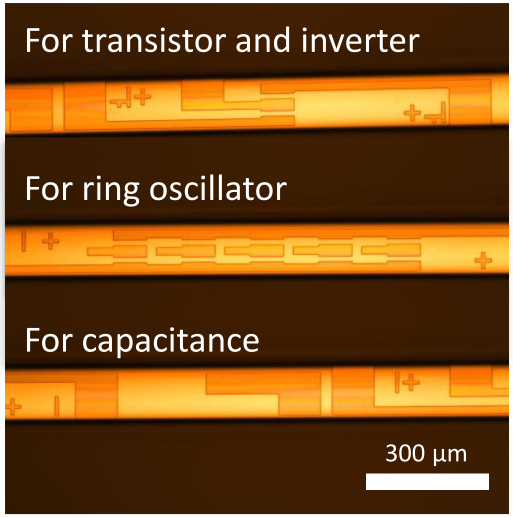
Electrodes and PR coating



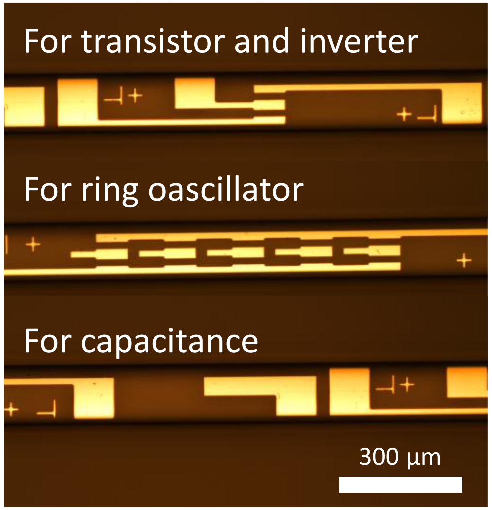




After Lithography and PR develop

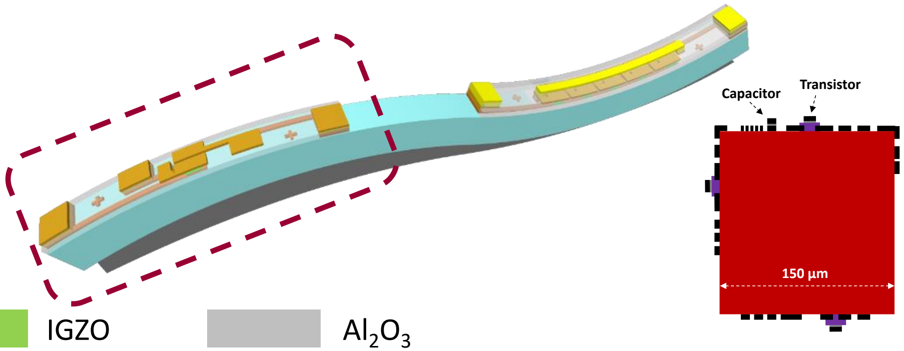


After wet-etching



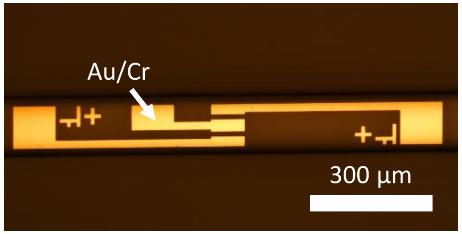
Chip on a fiber

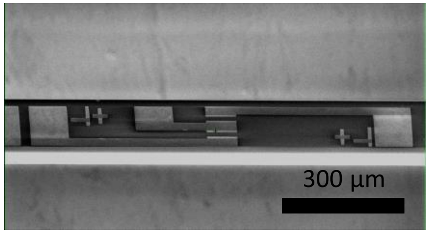
Transistor and inverter on fiber



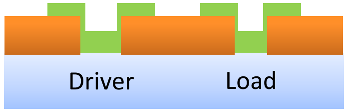
🟦 SiO$_2$ 🟧 Au/Cr 🟩 IGZO ⬜ Al$_2$O$_3$

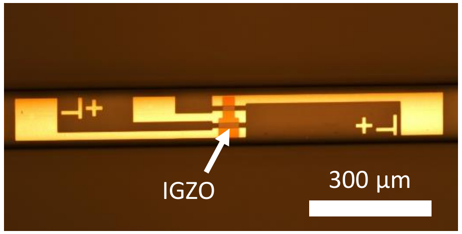
1. Au 30 nm /Cr 15 nm (Bottom electrodes)

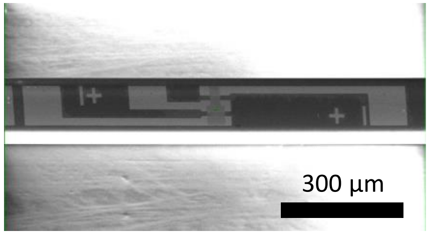




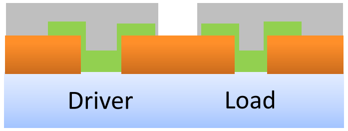
2. IGZO 15 nm (Active layer)

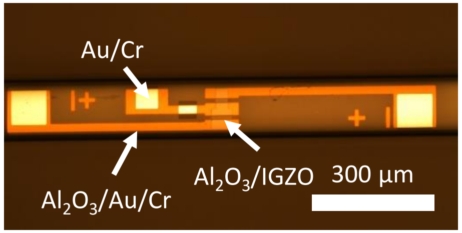


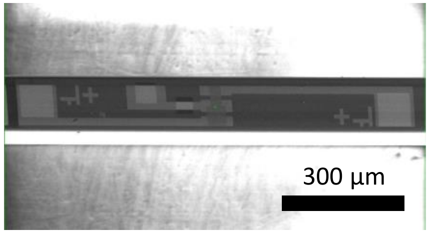




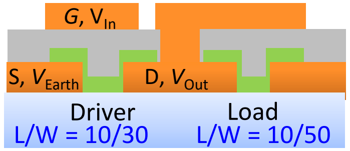
3. Al$_2$O$_3$ 36 nm (Dielectric layer)

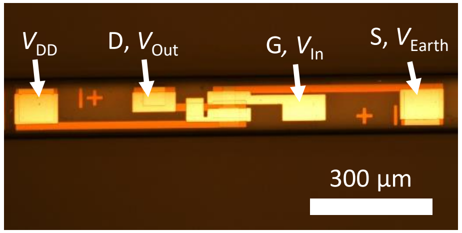


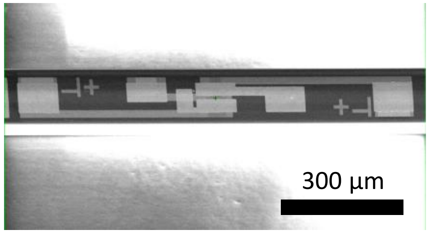




4. Au 30 nm /Cr 15 nm (Top electrodes)

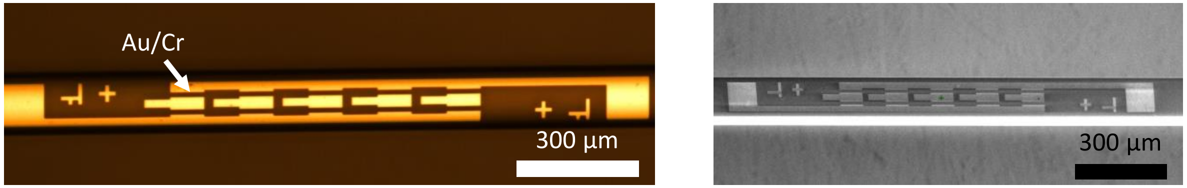




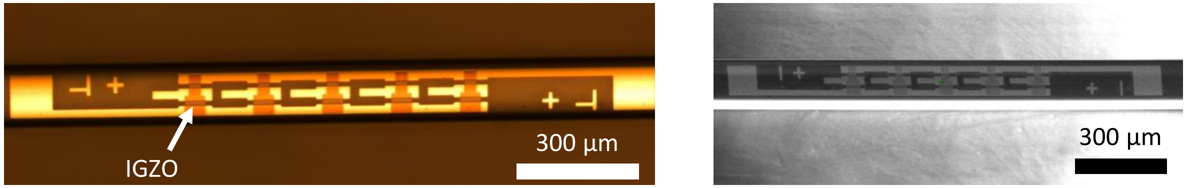


Chip on a fiber

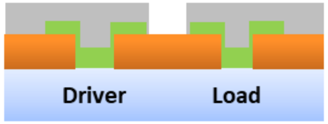
1. Au 30 nm /Cr 15 nm (Bottom electrodes)

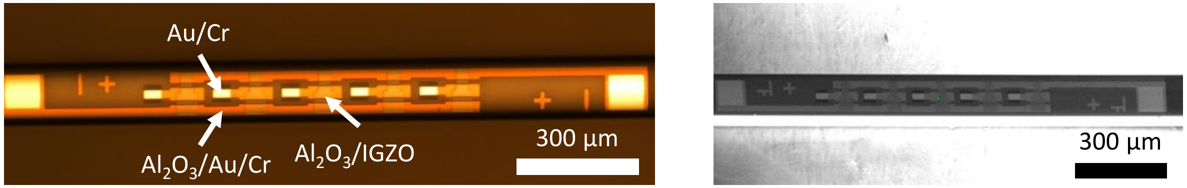


2. IGZO 15 nm (Active layer)

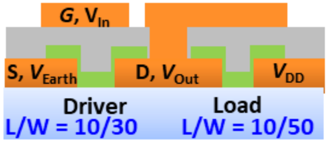


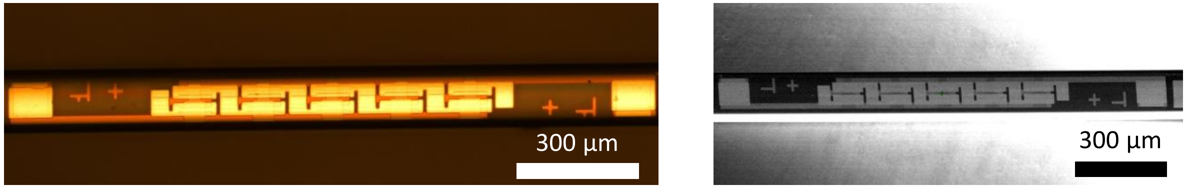
3. Al_2O_3 36 nm (Dielectric layer)



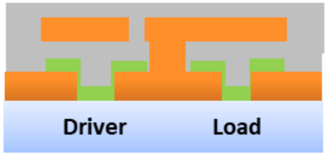


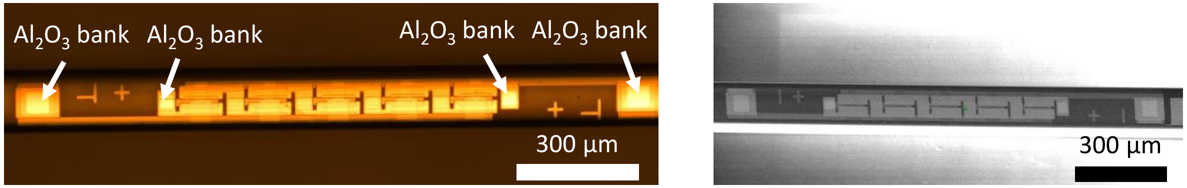
4. Au 30 nm /Cr 15 nm (Top electrodes)



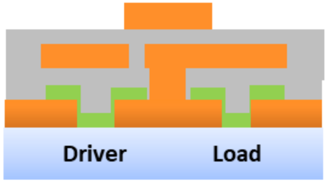


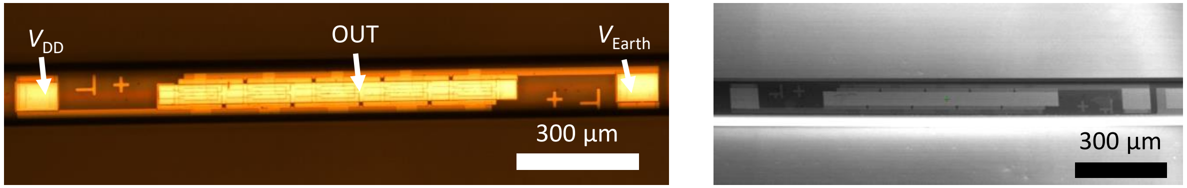
5. Al_2O_3 36 nm (Insulating layer)

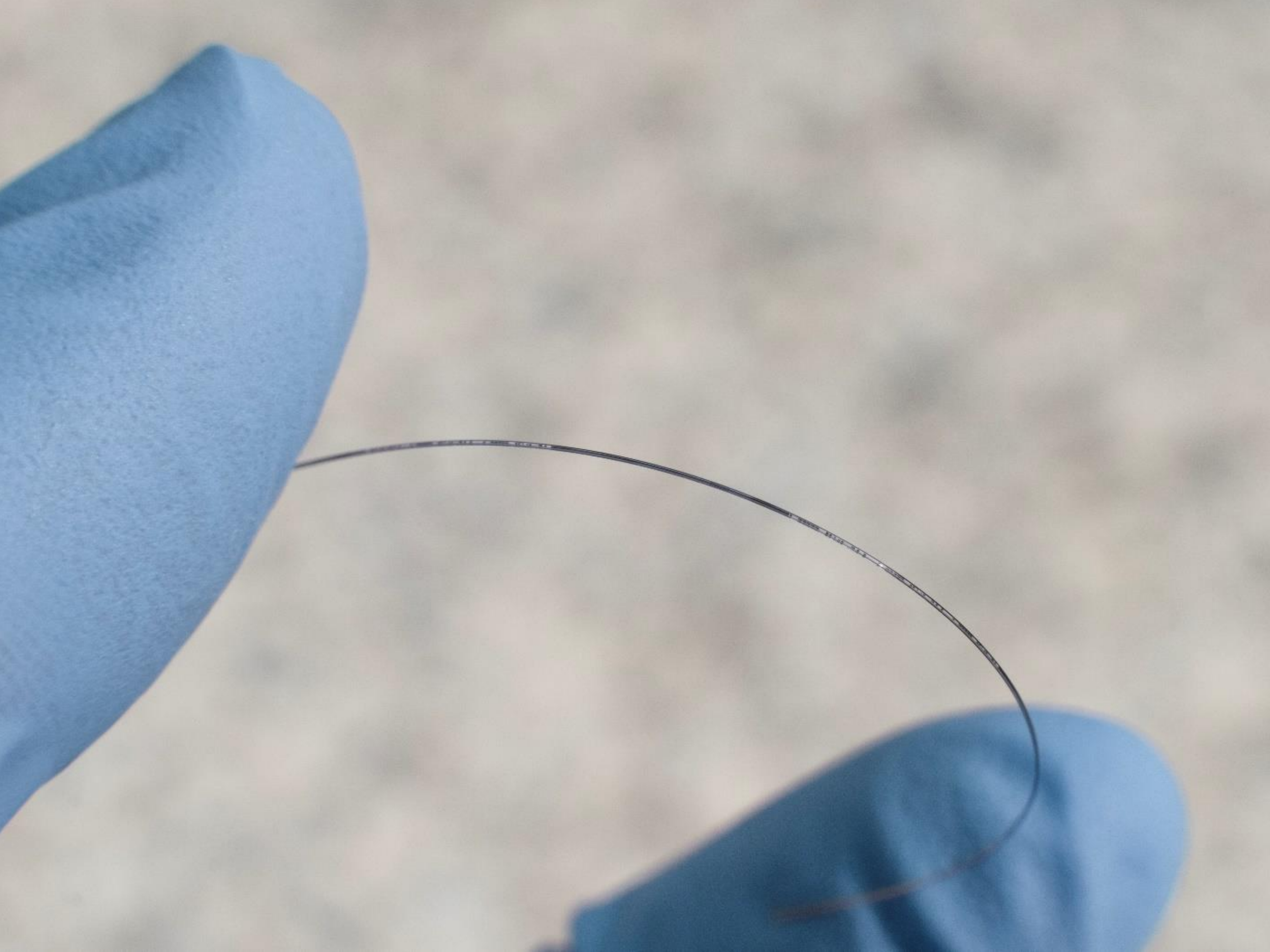




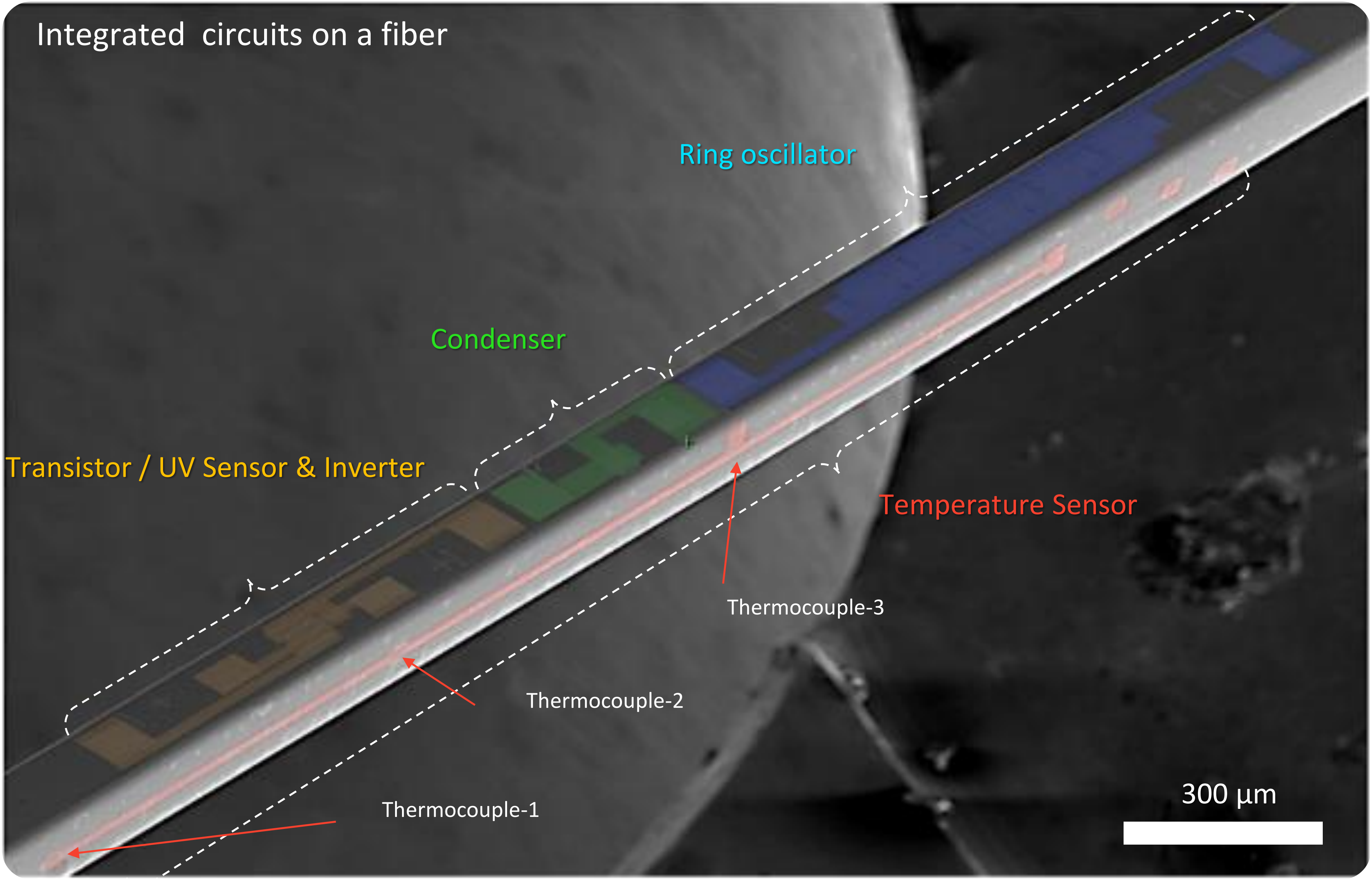
6. Au 30 nm /Cr 15 nm (1 to 5 stage connection)





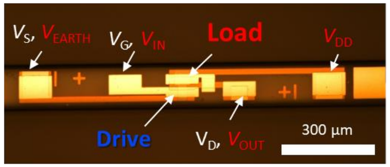


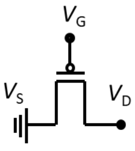
Chip on a Fiber



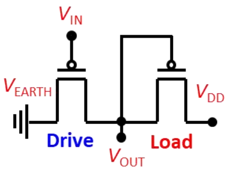
Chip on a fiber

- Transistor and inverter on a fiber substrate

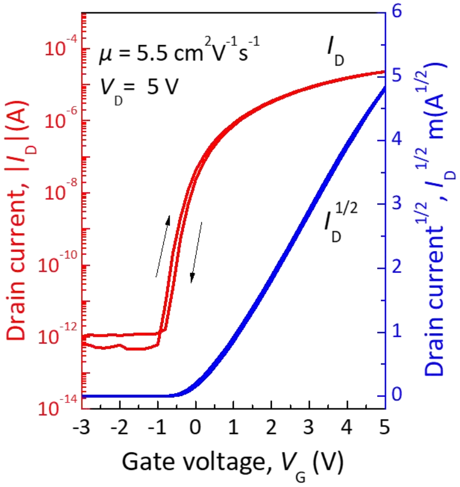


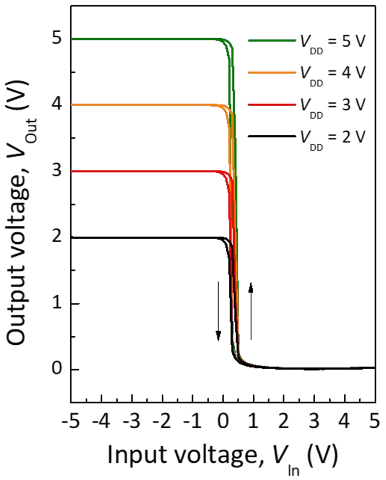


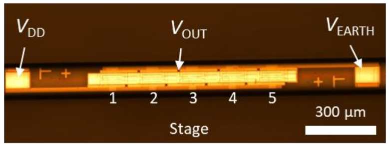
n-type
Transistor

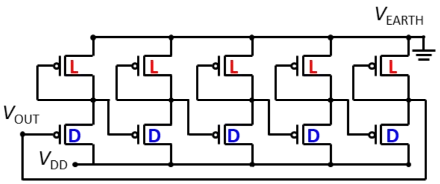


n-MOS depletion-mode
Inverter

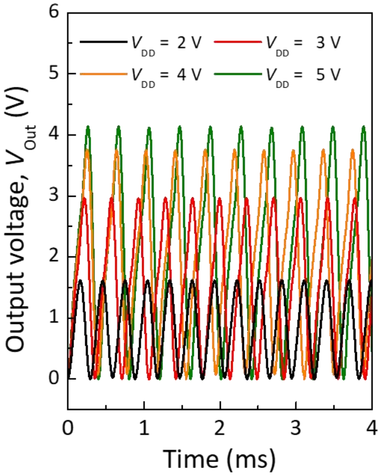


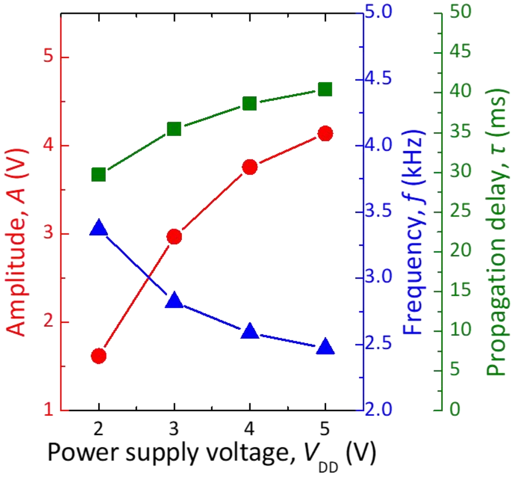






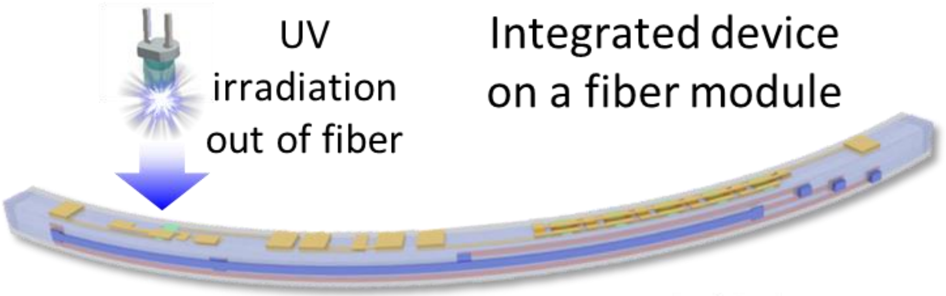
n-MOS depletion-mode
5 stage Ring oscillator

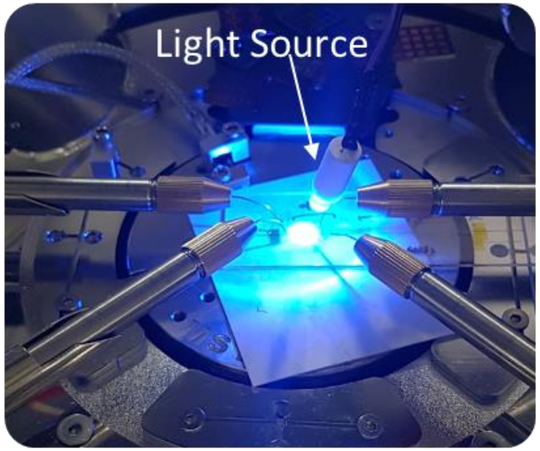


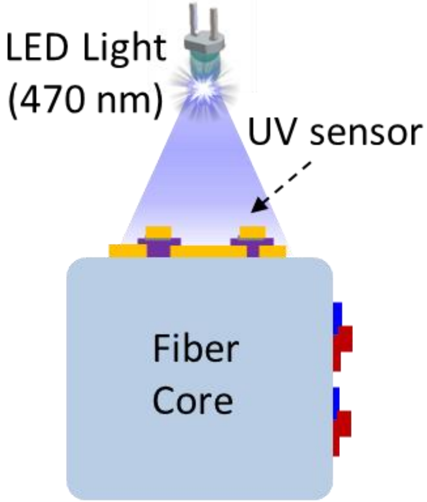


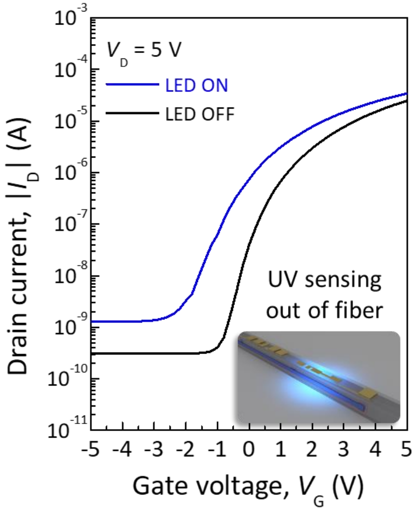
Chip on a fiber

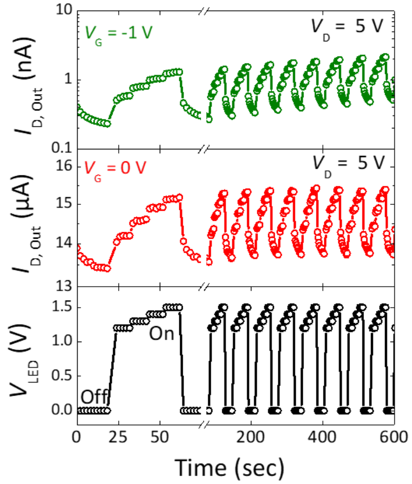
- Photo Detector (Light out of Fiber)





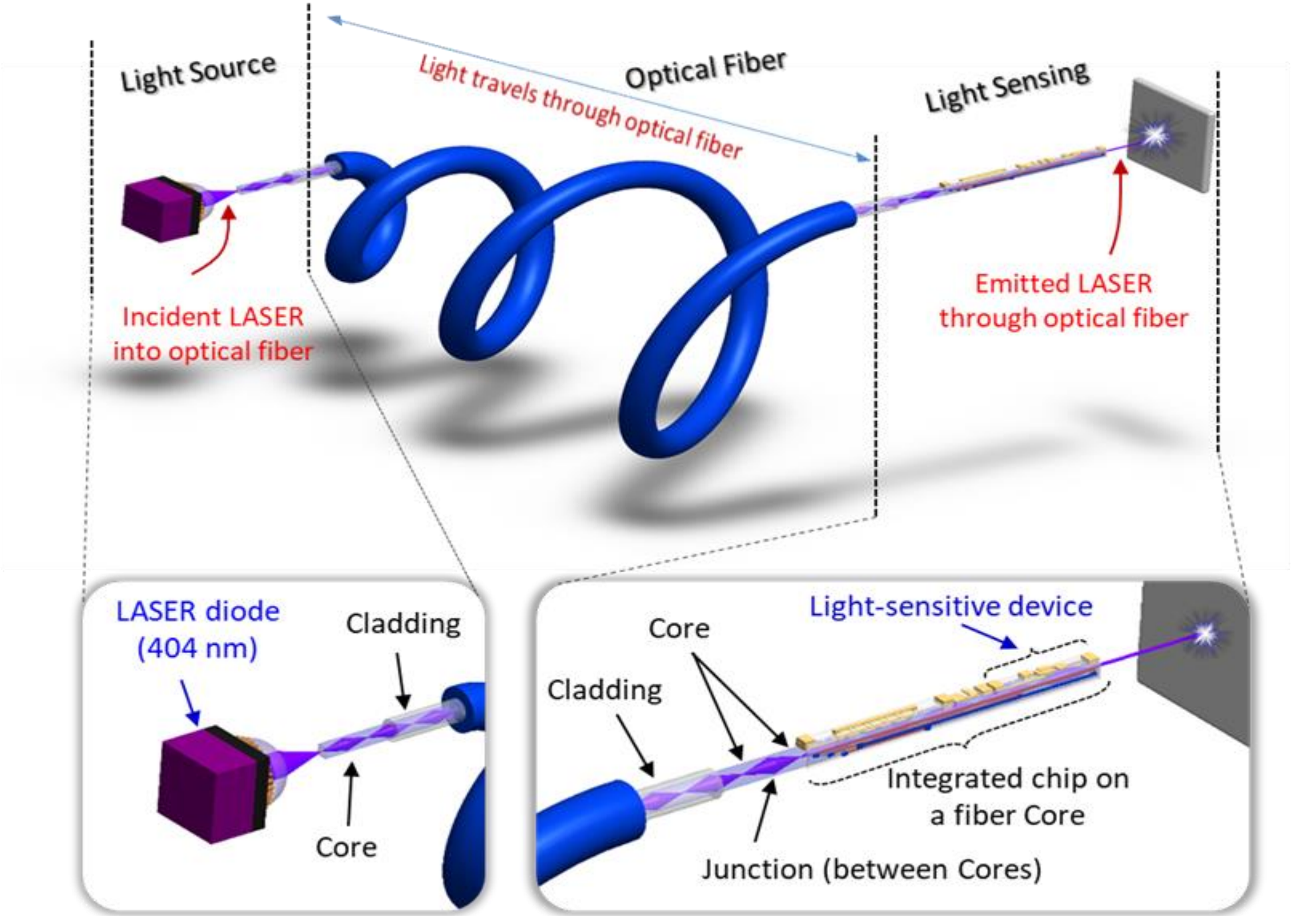


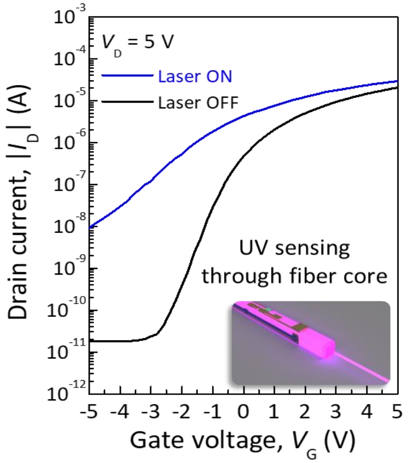


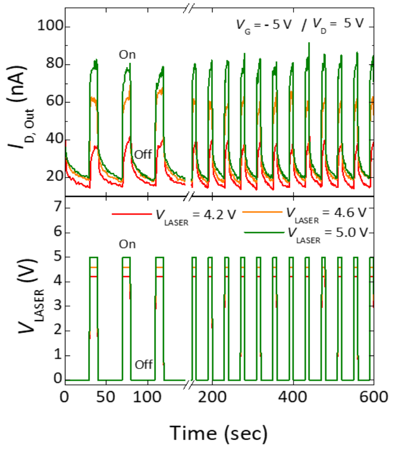


Chip on a fiber

- Photo Detector (Light through Fiber)

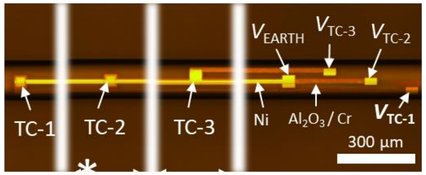




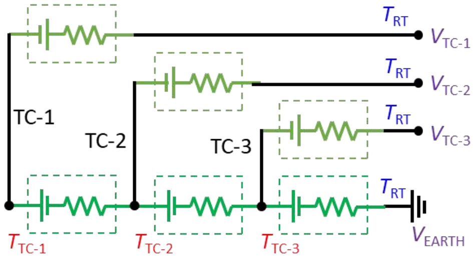


Chip on a fiber

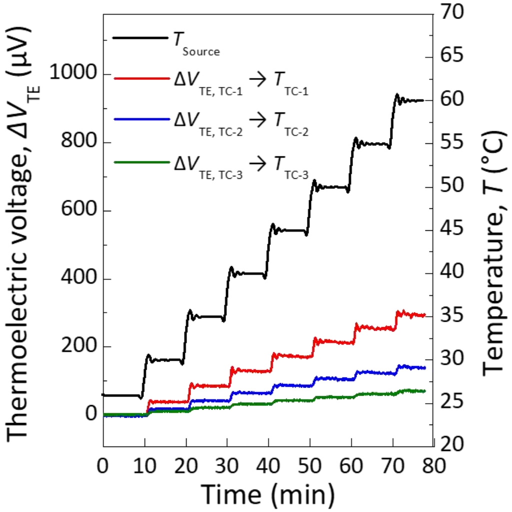
- Temperature sensor

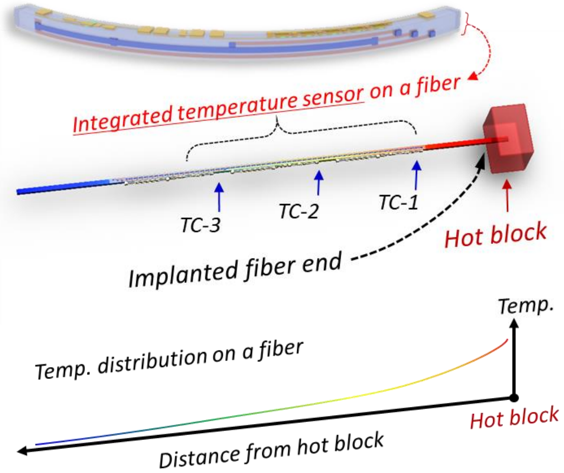


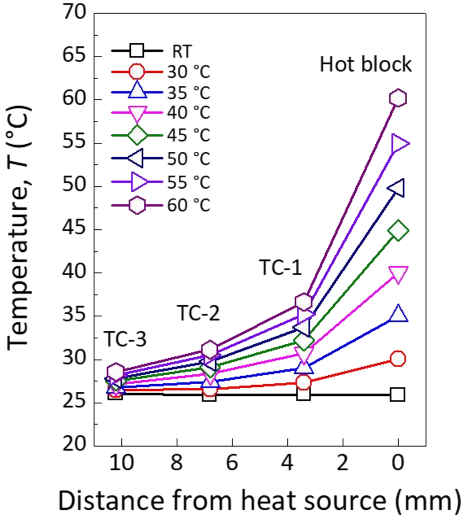
*Distance between each TCs is 3.4 mm



Cr-Ni Thermocouple column

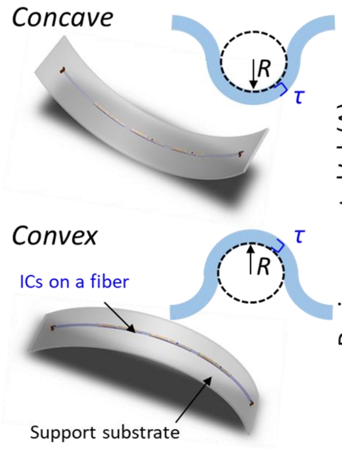


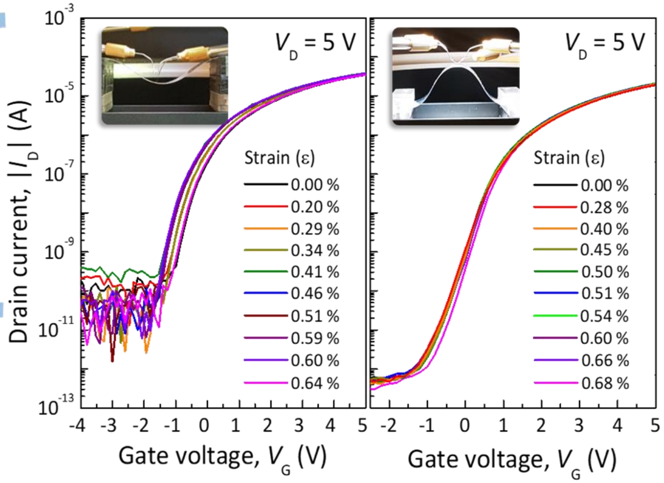


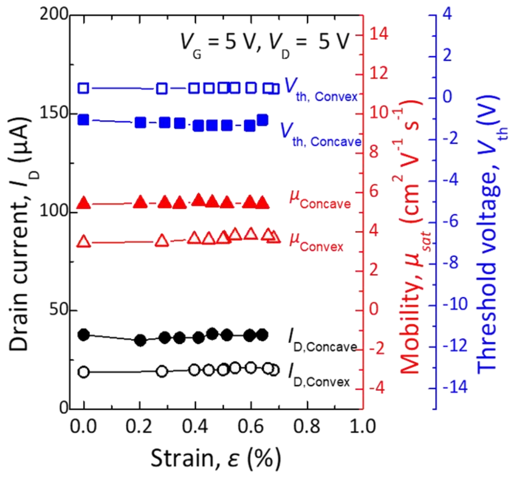


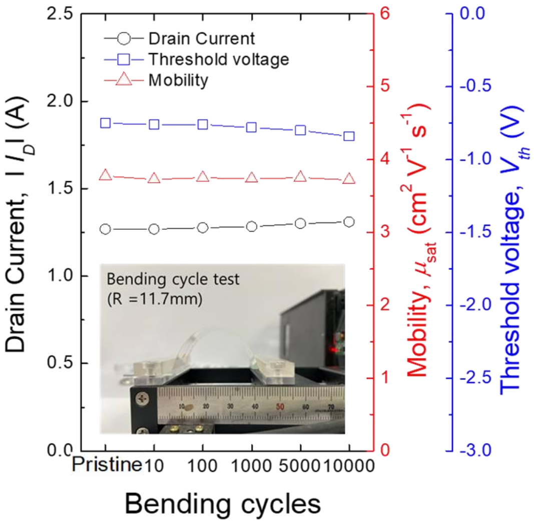
Chip on a fiber

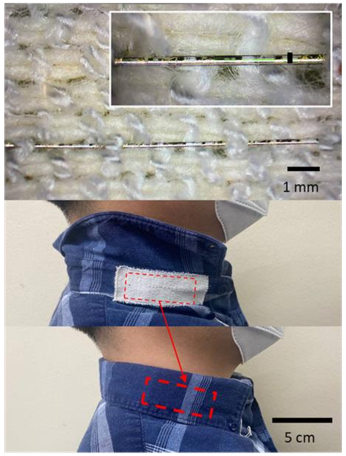
- Integrated electronic fiber under various bending conditions and embedding in a fabric

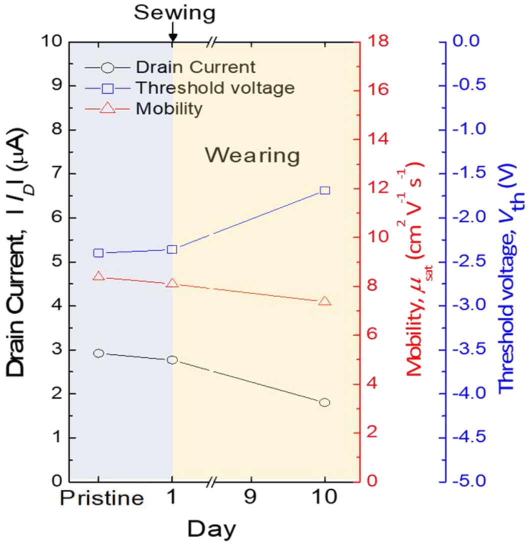












Pentium Processor vs. Processor on a Fiber

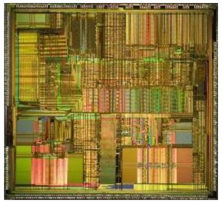
Code name: P54CS

Clock speed: 200 MHz

Introduce: 1996-6-10

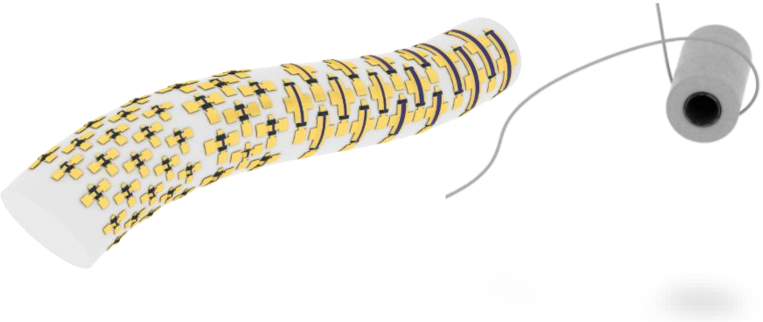
Process size: 0.35 µm

Number of Transistor: 3.3 millions



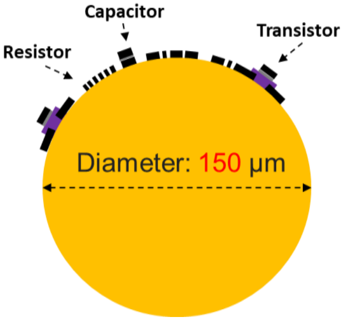
Die area: 91mm^2

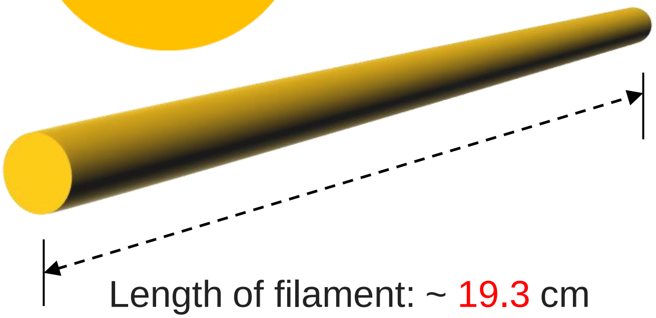
=



Process size: 0.35 µm

Number of Transistor: 3.3 millions

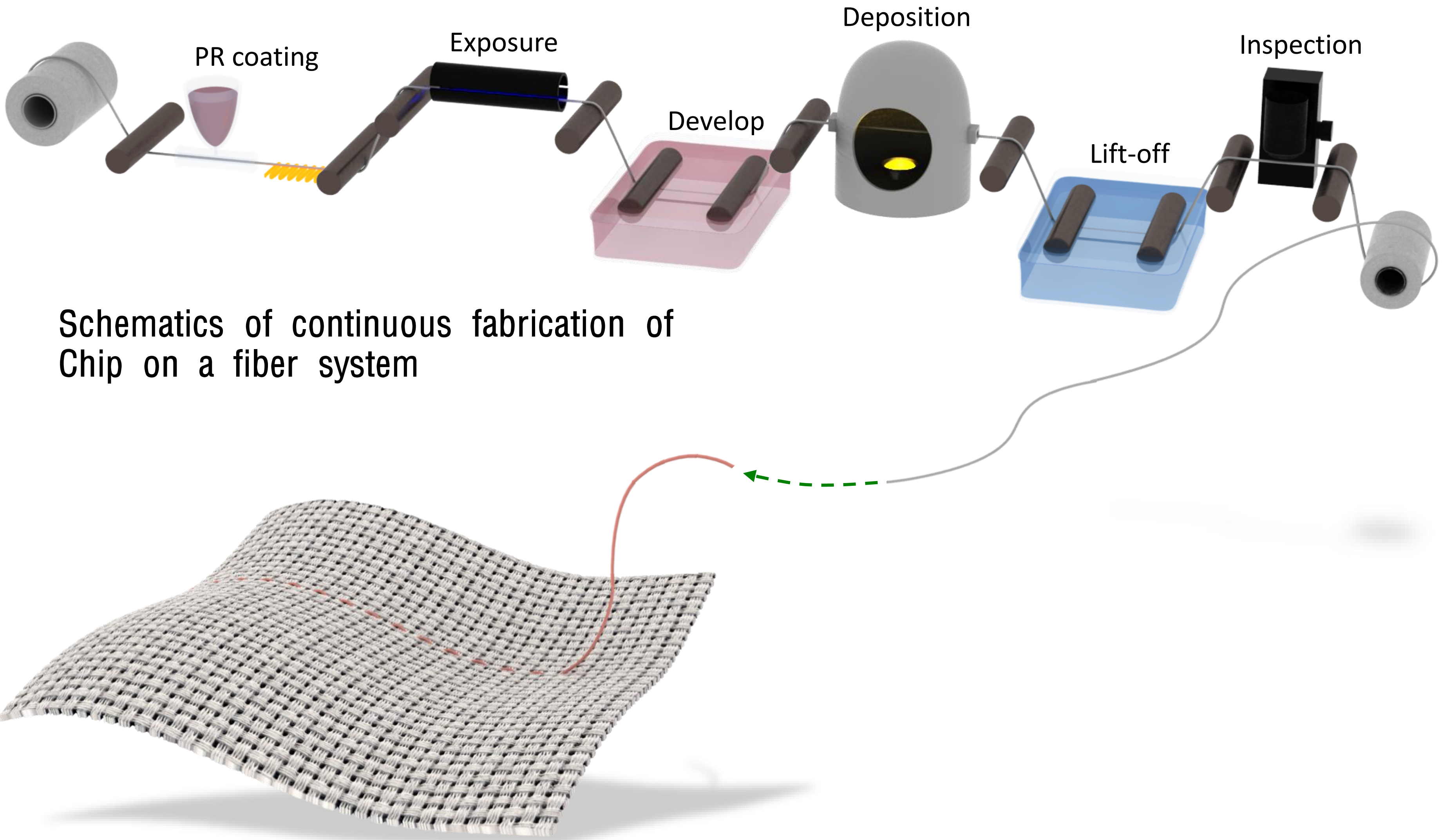




Length of filament: ~ 19.3 cm

Hwang et al, *Nature Communications*, 13 (1), 1-10 (2022)

Chip on a Fiber

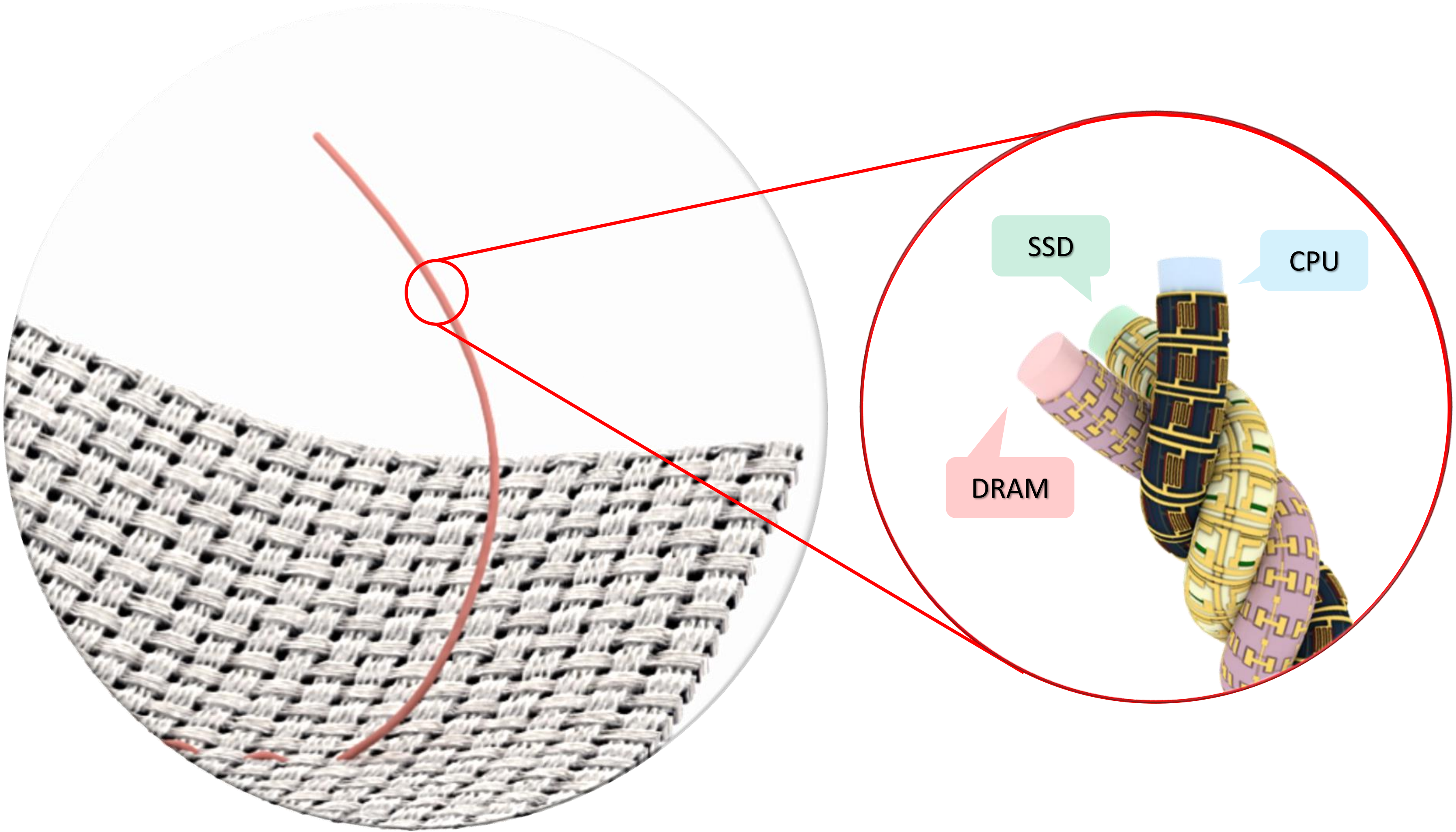


Schematics of continuous fabrication of Chip on a fiber system

Chip on a fiber(filament) system for wearable processor, memory, sensor

Chip on a fiber

"Fiber computing module based on New E-textile platform"



Toward next generation

E-Textile

Summary

Keep thinking for new idea

End of Slide