Engineering of Semiconductor

:Semiconductor Physics and Devices

Chapter 2. Silicon Technology

Objectives

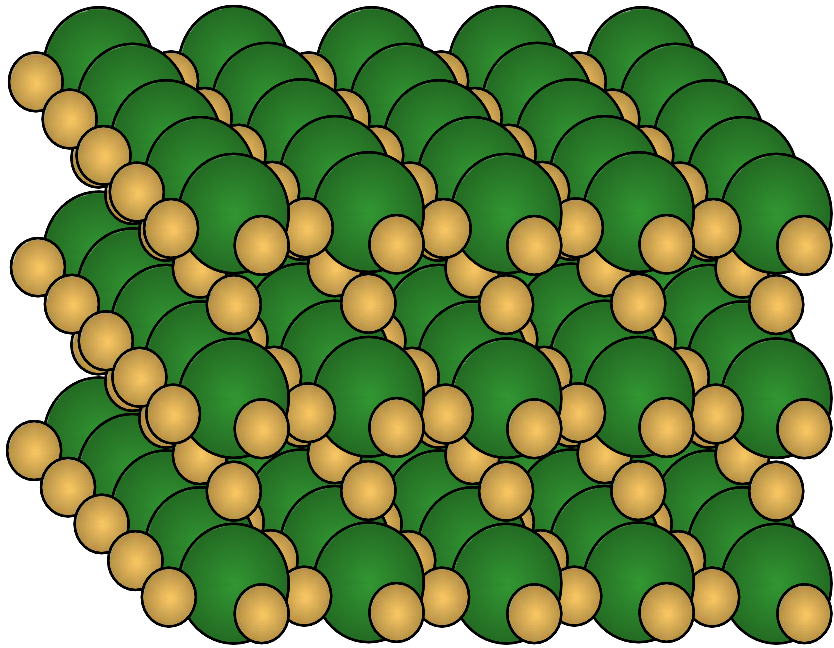
Overview of Silicon Technology

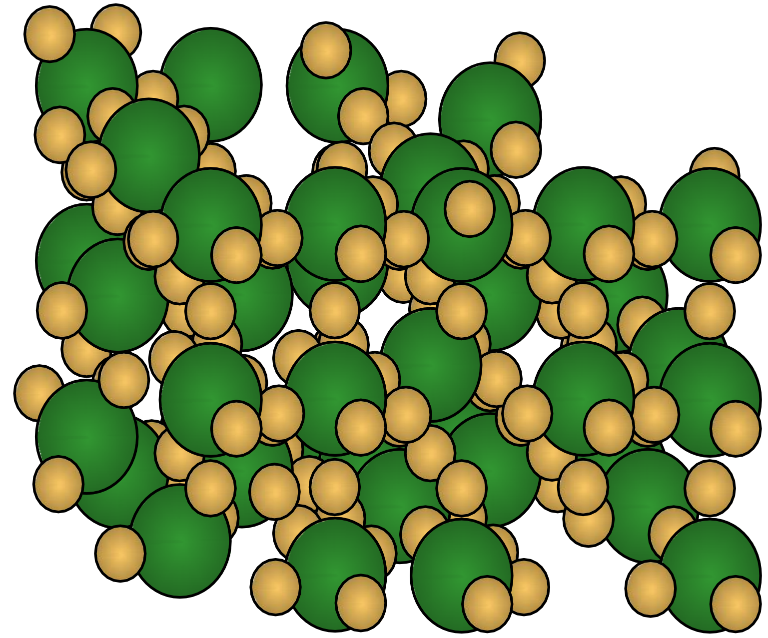
- Wafer preparation
- Oxidation
- Lithography
- Etching
- Doping
- Deposition
- Packaging

Semiconductor-Grade Silicon

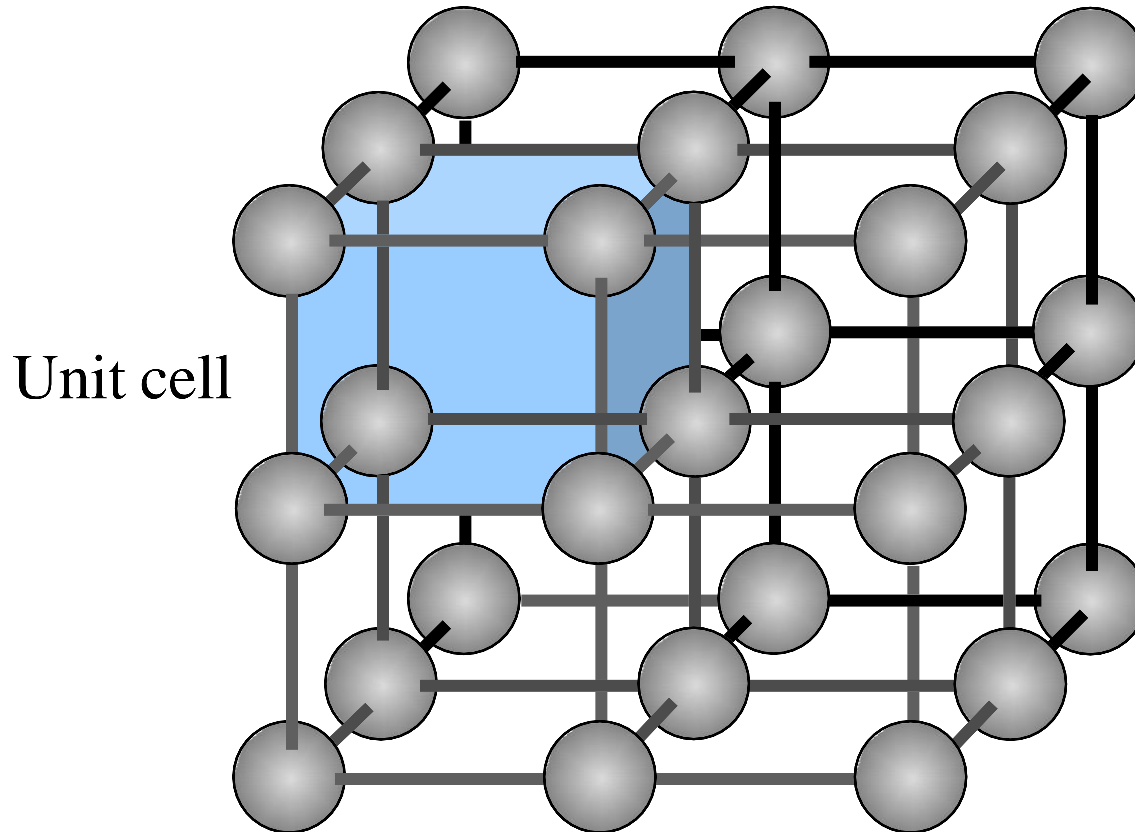
Steps to Obtaining Semiconductor Grade Silicon (SGS)		
Step	**Description of Process**	**Reaction**
1	Produce metallurgical grade silicon (MGS) by heating sil ica with carbon	SiC (s) + SiO_2 (s) → Si (l) + SiO(g) + CO (g)
2	Purify MG silicon through a chemical reaction to produce a silicon-bearing gas of trichlorosilane ($SiHCl_3$)	Si (s) + 3HCl (g) → $SiHCl_3$ (g) + H_2 (g) + heat
3	$SiHCl_3$ and hydrogen react in a process called Siemens to obtain pure semiconductor-grade silicon (SGS)	$2SiHCl_3$ (g) + $2H_2$ (g) → 2Si (s) + 6HCl (g)

Atomic Order of a Crystal vs. Amorphous Structure





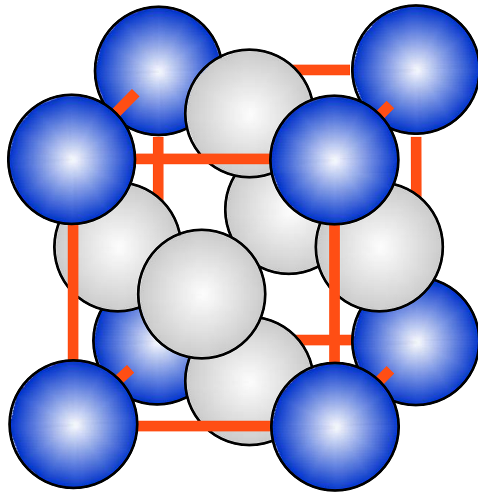
Unit Cell in 3-D Structure



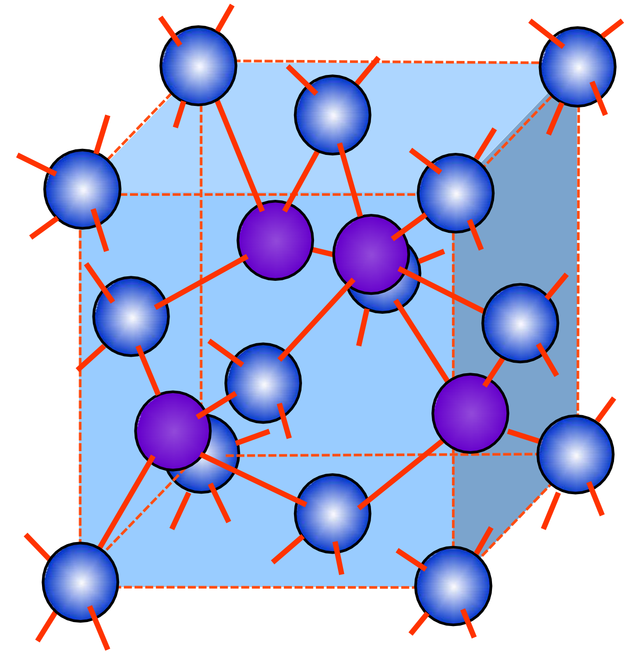
the smallest portion of a crystal lattice that shows the three-dimensional pattern of the entire crystal

Polycrystalline and Monocrystalline Structures

Faced-centered Cubic (FCC) Unit Cell

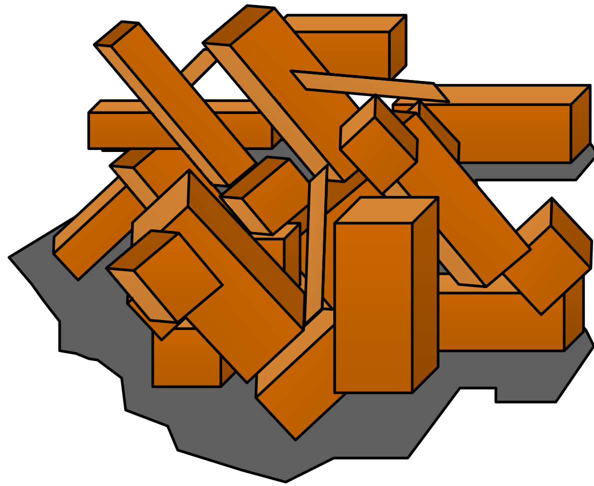


Silicon Unit Cell: FCC Diamond Structure

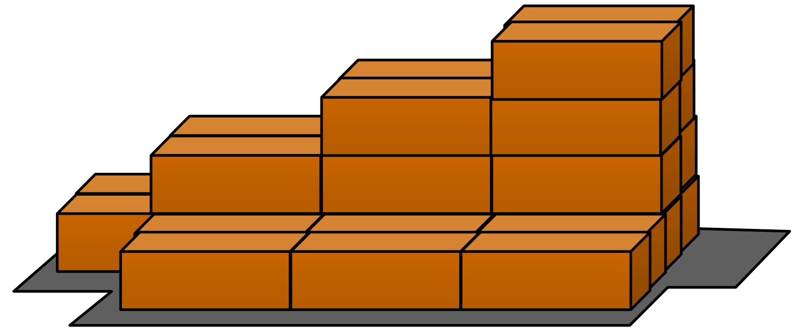


Crystalline structure of Silicon

Polycrystalline structure

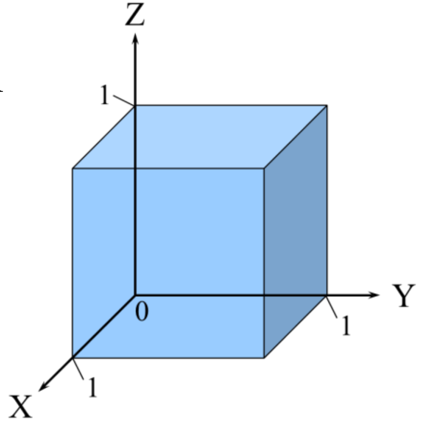


Monocrystalline structure



Axes of Orientation for Unit Cells

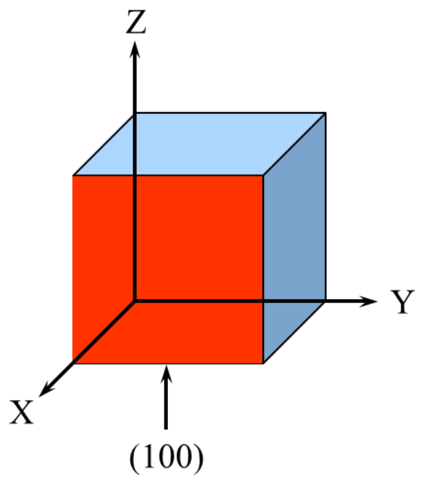
Unit cell

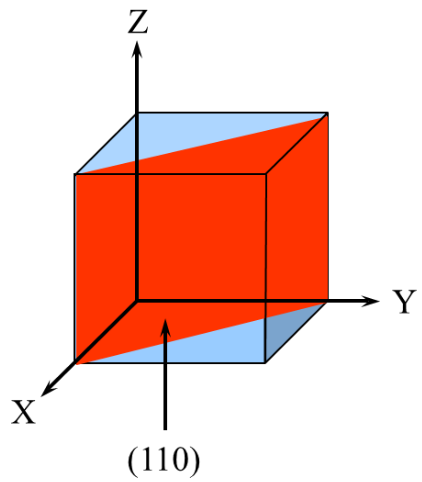


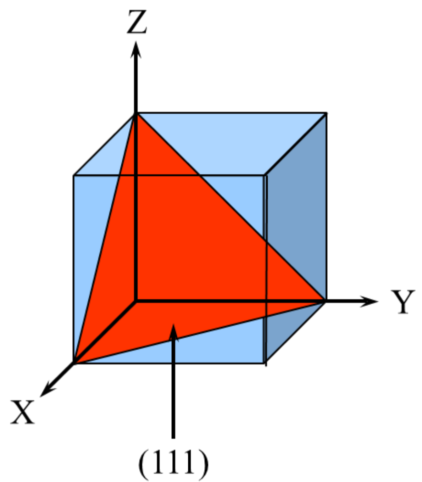
Miller indices form a notation system in crystallography for planes in crystal (Bravais) lattices

Homework "Miller Index"

Miller Indices of Crystal Planes





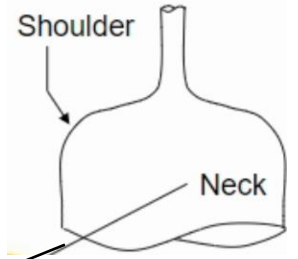


Growth of singlecrystal Silicon

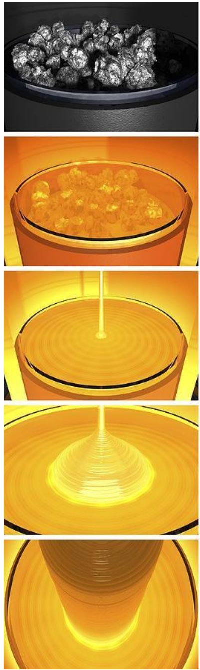
- CZ Method
  - CZ Crystal Puller
  - Doping
  - Impurity Control
- Float-Zone Method
- Reasons for Larger Ingot Diameters

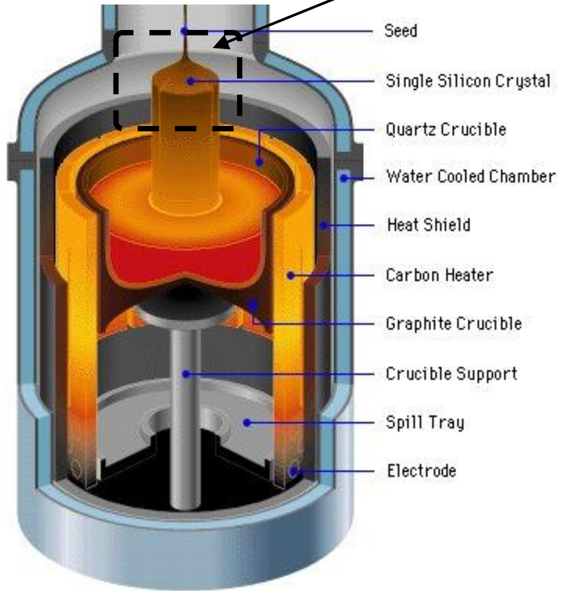
Czochralski (CZ) method

The Czochralski (CZ) method is a crystal growth technology that starts with insertion of a small seed crystal into a melt in a crucible, pulling the seed upwards to obtain a single crystal.



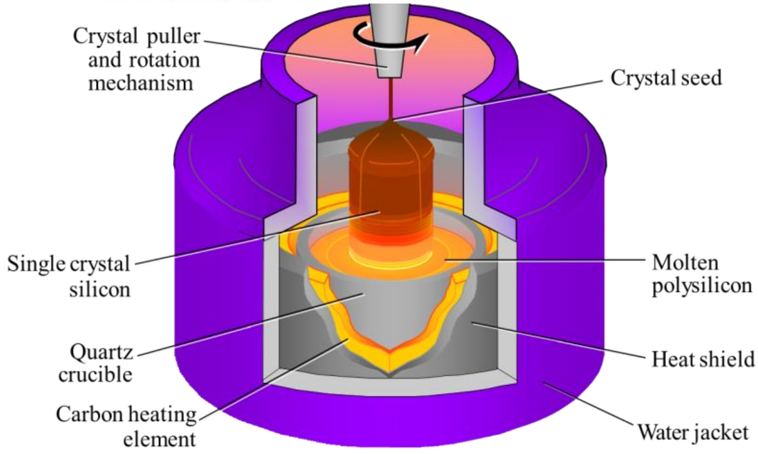
- In 1918, Czochralski developed process.
- Polycrystal Si → single crystal Si
- Single crystal is pulled from a melt.
- Orientation of seed determine the orientation of Si wafer.





[Process]

- Melting of P-Si in quartz crucible
- Deep the crystal seed in to the Si melt
  *Crystal growth at the interface of melt following the crystallographic structure of seed
- Seed rotation + pulled-up from the melt
  fast speed (necking, defect ↓)
  → slow speed (shoulder, diameter ↑)
- Growth (Ingot)
- Increase pull speed (ingot diameter & thermal shock ↓)



Czochralski (CZ) method

CZ Crystal Puller

Photograph courtesy of Kayex Corp., 300 mm Si crystal puller

Czochralski (CZ) method

https://www.youtube.com/watch?v=2qLI-NYdLy8&t=141s

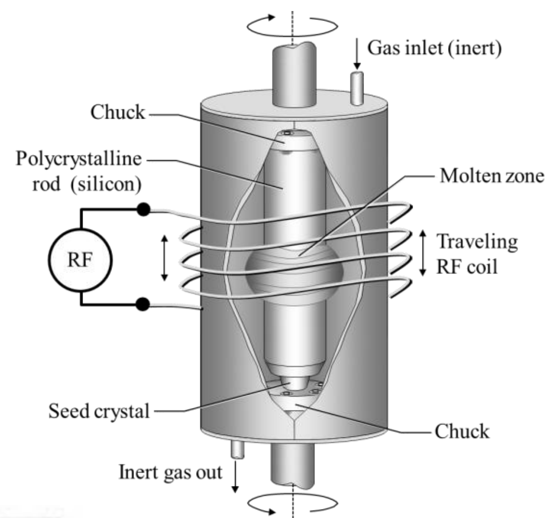
Czochralski (CZ) method

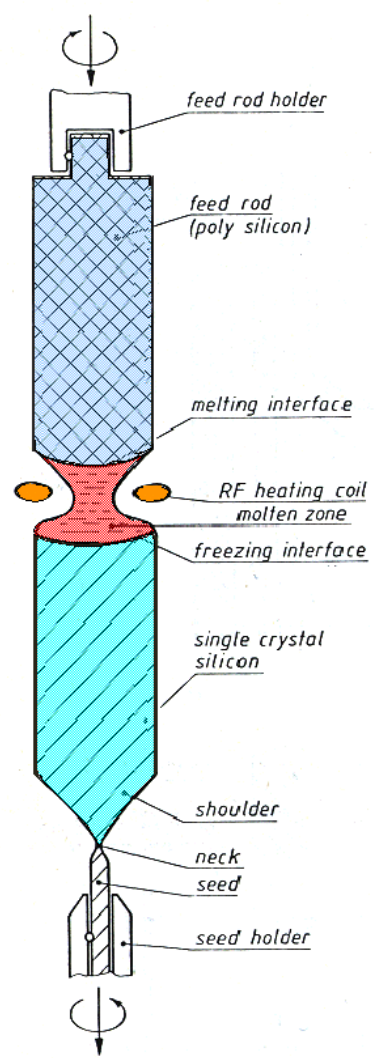
Dopant Concentration Nomenclature

		Concentration (Atoms/cm^3)			
Dopant	**Material Type**	$< 10^{14}$ (Very Lightly Doped)	10^{14} to 10^{16} (Lightly Doped)	10^{16} to 10^{19} (Doped)	$>10^{19}$ (Heavily Doped)
Pentavalent	n	n^{--}	n^{-}	n	n^{+}
Trivalent	p	p^{--}	p^{-}	p	p^{+}

Float Zone Crystal Growth method

Schematics of Float Zone crystal growth





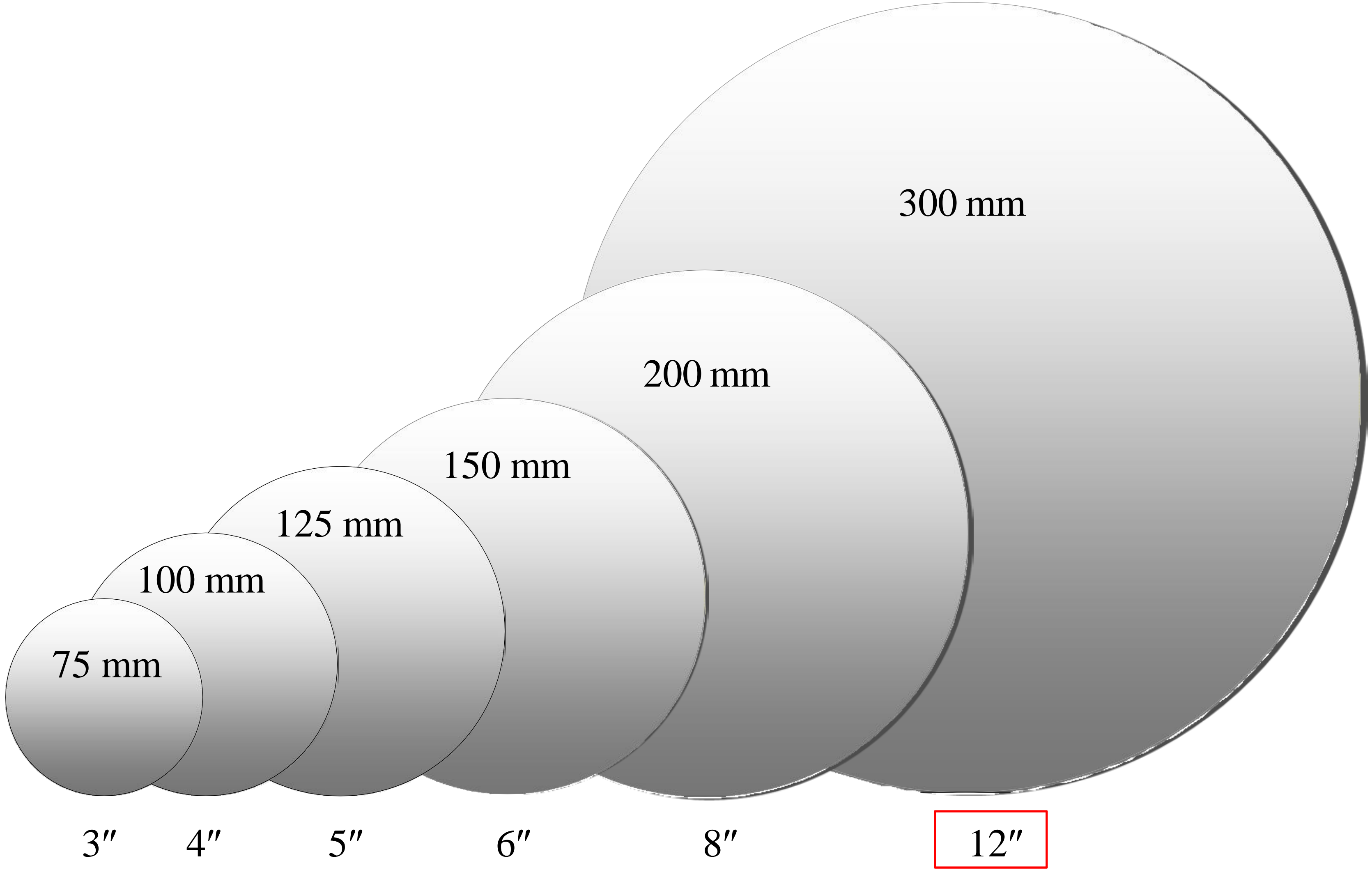
a)
sintered rod
molten zone
sintered rod

b)
sintered rod
molten zone
larger grains
sintered rod

c)
sintered rod
molten zone
single crystal
larger grains
sintered rod

d)
sintered rod
molten zone
single crystal
larger grains
sintered rod

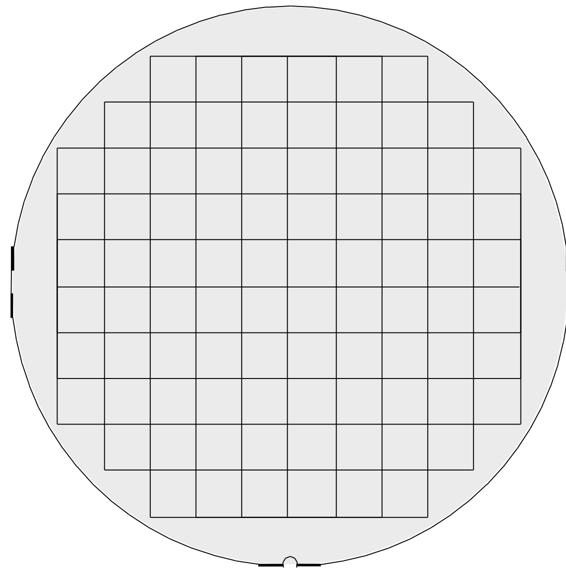
Wafer Diameter Trends for Silicon



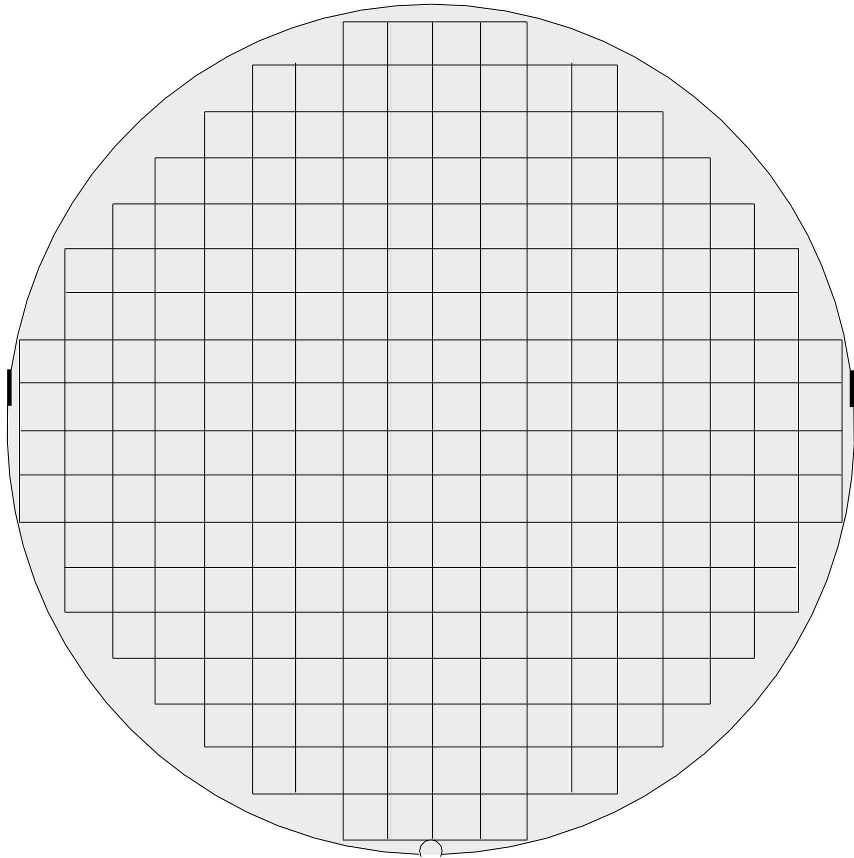
Samsung, SK Hynix

Why larger wafer?

Increase in Number of Chips on Larger Wafer Diameter



88 die
200-mm wafer



232 die
300-mm wafer

Crystal Defects in Silicon

A crystal defect (*microdefect*) is any interruption in the repetitive nature of the unit cell crystal structure.

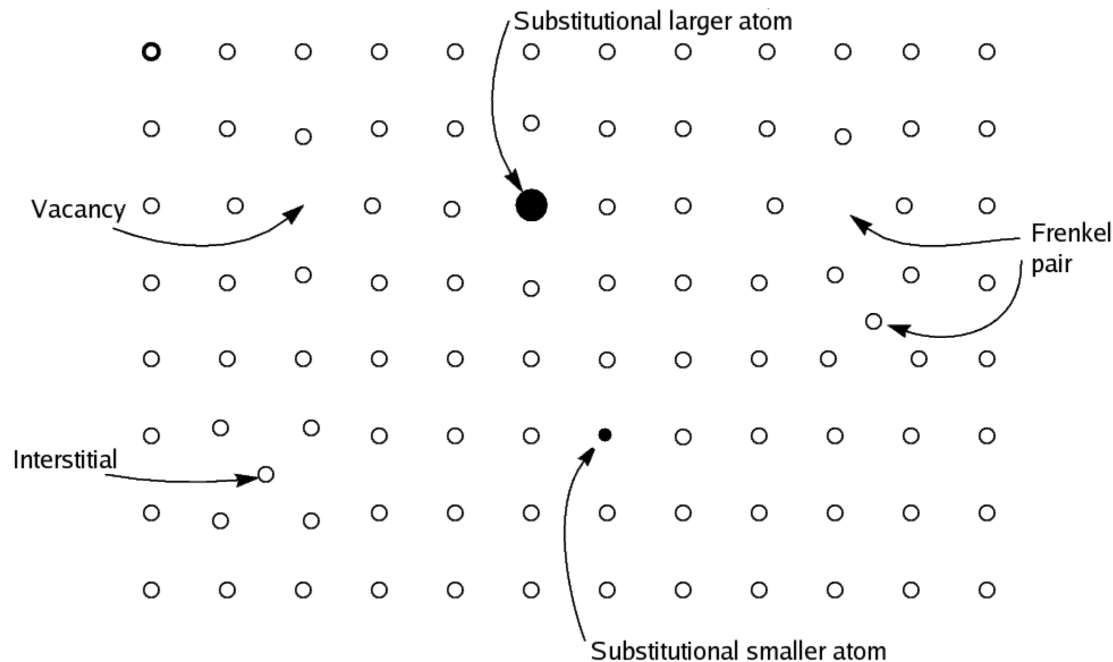
Three general types of crystal defects in silicon:

1. Point defects: Localized crystal defect at the atomic level
2. Dislocations: Displaced unit cells

Crystal Defects in Silicon

Point defects

Point defects are defects that occur only at or around a single lattice point



Vacancy defects are lattice sites which would be occupied in a perfect crystal, but are vacant

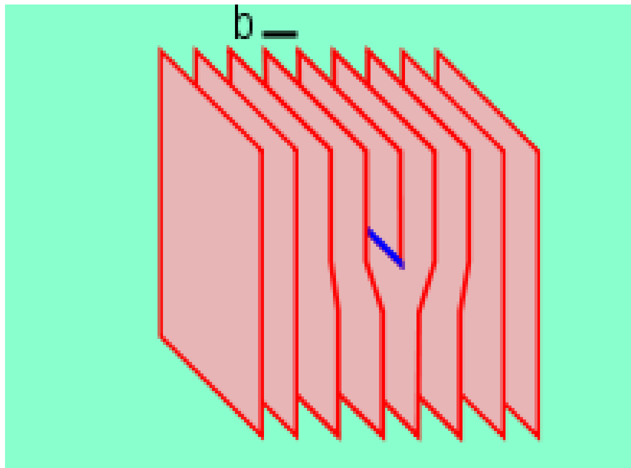
Interstitial defects are atoms that occupy a site in the crystal structure at which there is usually not an atom

Frenkel defect: A nearby pair of a vacancy and an interstitial

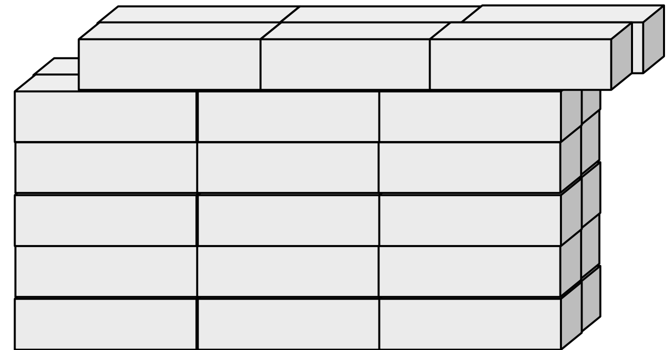
Crystal Defects in Silicon

Dislocations

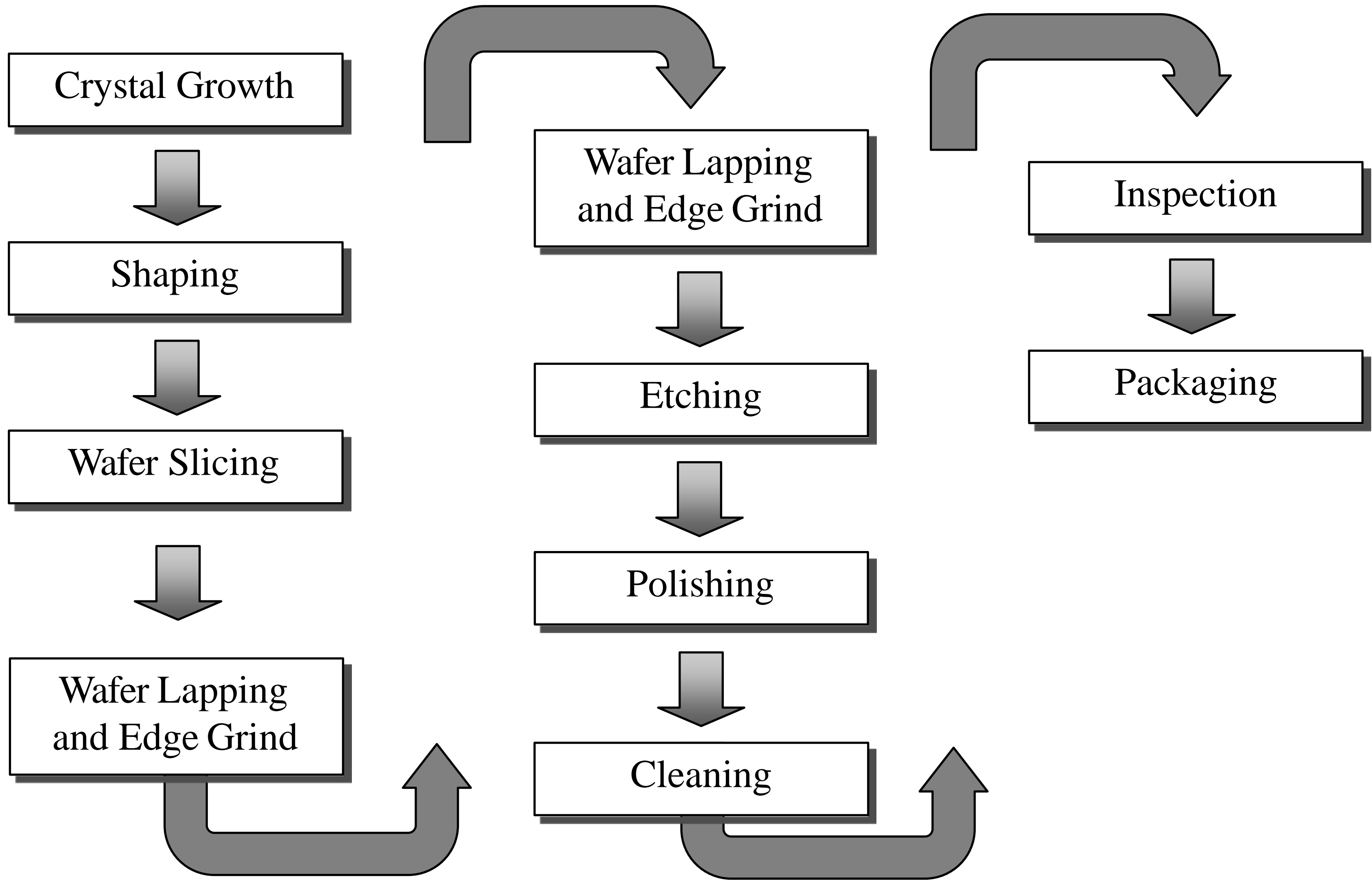
Dislocations are linear defects, around which the atoms of the crystal lattice are misaligned



Dislocations in Unit Cells

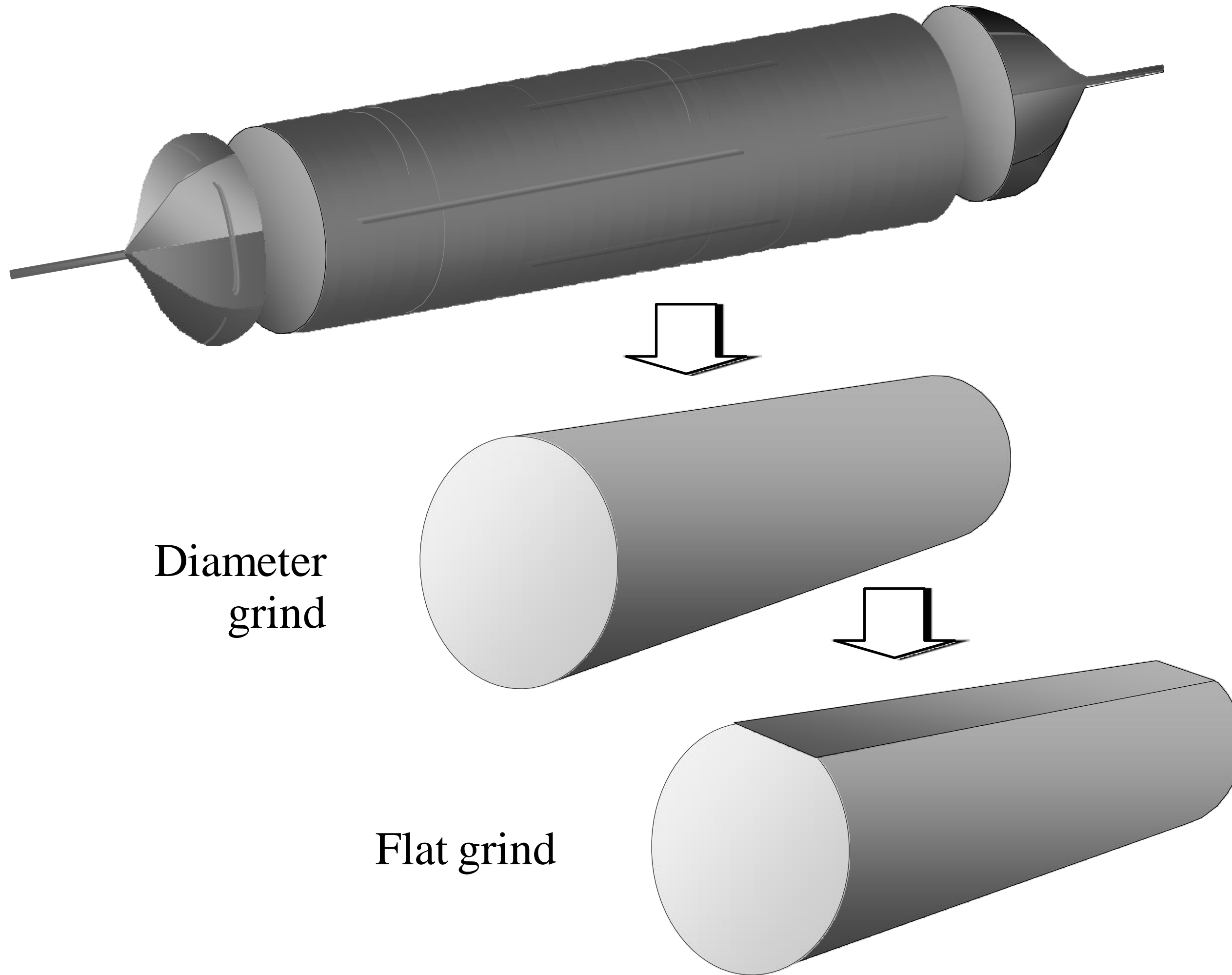


Basic Process Steps for Wafer Preparation



Ingot Diameter Grind

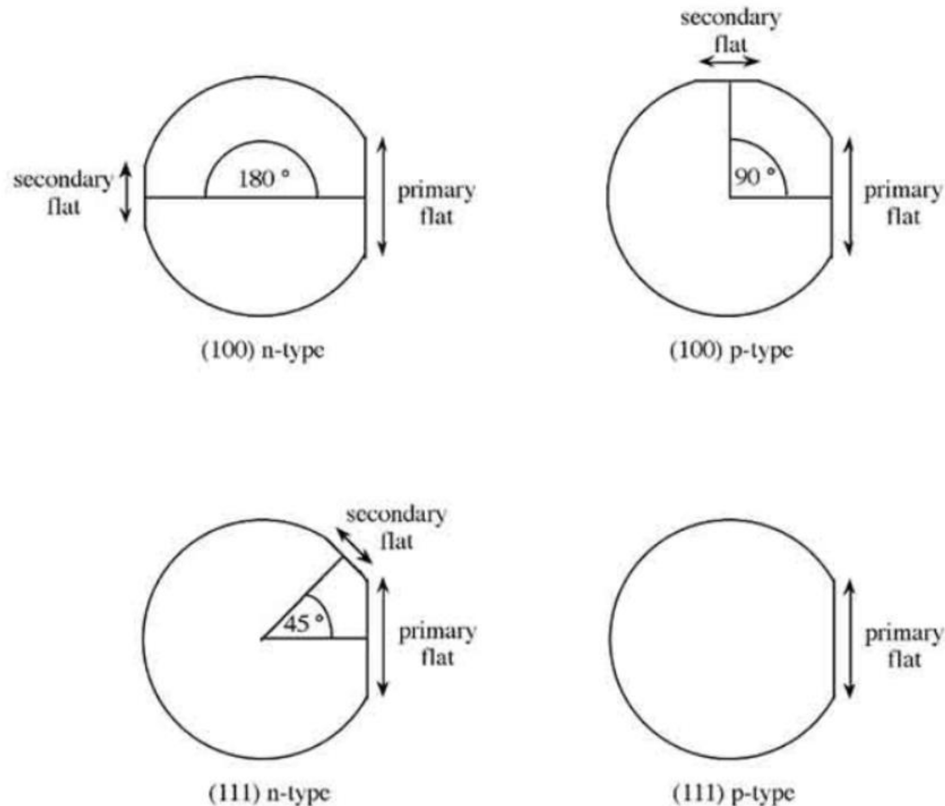
Preparing crystal ingot for grinding

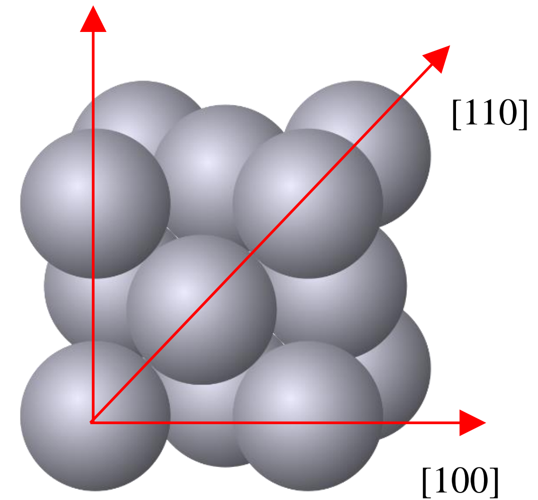


Wafer Identifying Flats

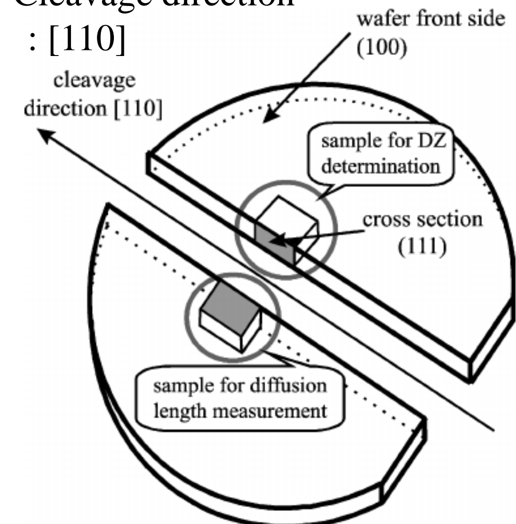
Silicon wafer

-Round-shaped + flat
-Size : 2in, 4in, 6in, 8in ~ 18in
- Type : <100>,<110>,<111>





- Cleavage direction : [110]



Oxidation
Dry 3000A#1

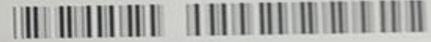
QL

Polished Wafer(PRIME)

SPEC NUMBER:	/	GROWTH METHOD:	CZ
ORIENTATION:	<100> 0°±1°	THICKNESS:	675±25um
TYPE/DOPANT:	P/B	DIAMETER:	150.0±0.2mm
RESISTIVITY:	<0.005 Ω.cm	PACKING DATE:	20/11/14

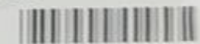
(P)PART NUMBER: /

(7Q)QUANTITY: 25



(1T)LOT#: 6BL05GZ0

(1V)VENDER: QL



BACK SURFACE:

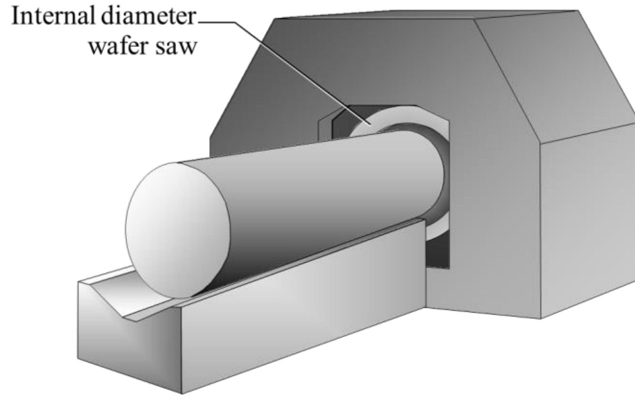
SN

6BL05GZ0-1

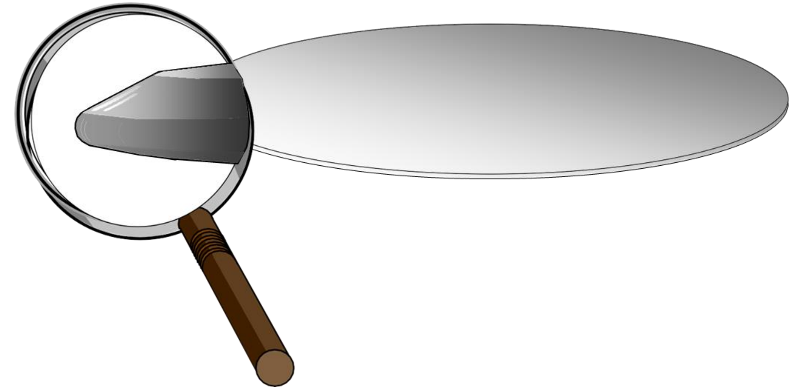
25

Wafer preparation

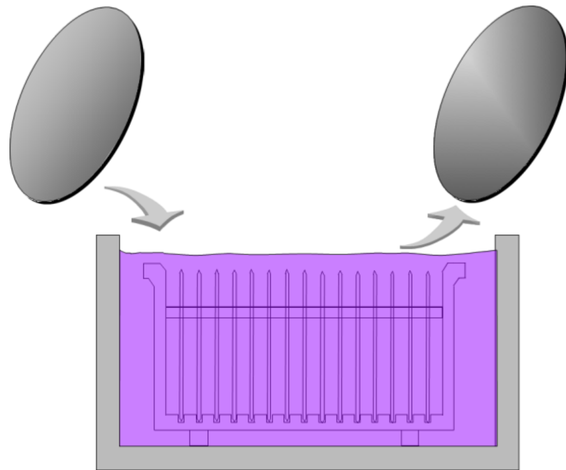
Internal Diameter Saw



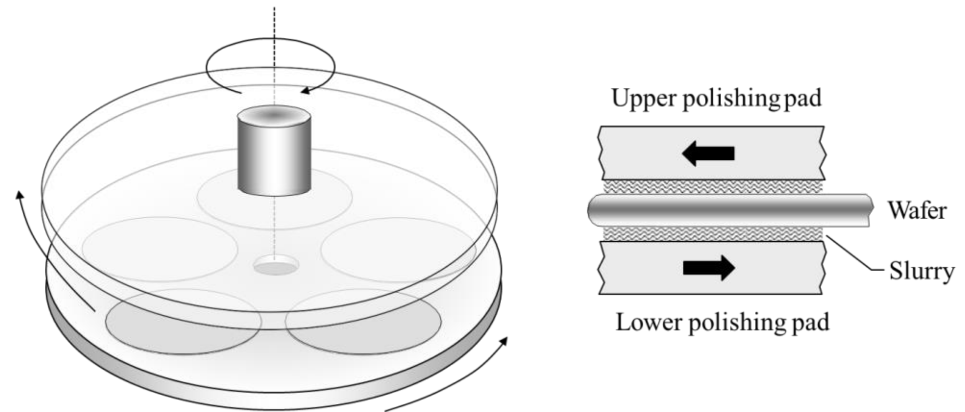
Polished Wafer Edge



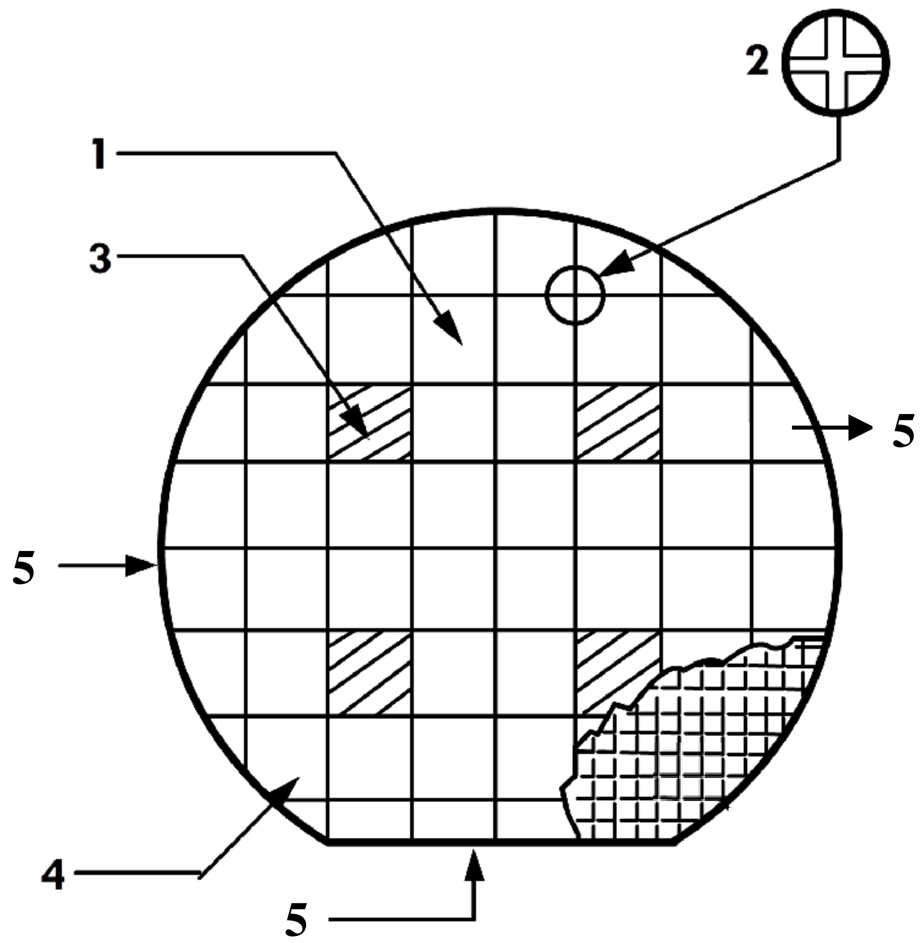
Chemical Etch of Wafer Surface to Remove Damage



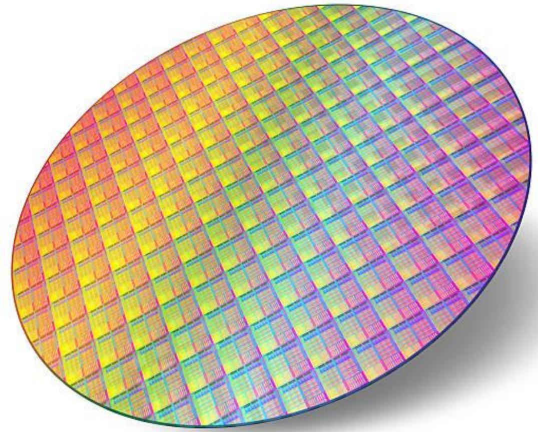
Double-Sided Wafer Polish



Terminology of wafer

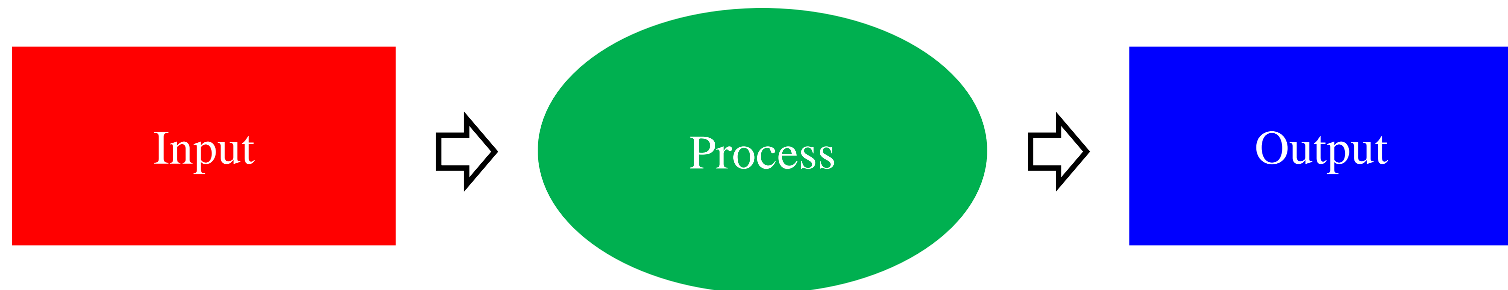


1. Chip, Die, Device
2. Scribe line
3. Test element group (TEG)
4. Edge die
5. Flat zone



Yield

- Opposite of defective rate
- Output / Input
- Division of Yield
  : 4 Group – Fabrication, Probe, Package, Test
- Total Yield (CUM Yield) : ($Y_{fab.}$) x (Y_{prove}) x ($Y_{package}$) x (Y_{test})



Wafer processing

- Classification of wafer processing

Class	Purpose	Technique.
Thin film deposition	Formation of thin film on wafer	Oxidation : atmospheric pressure CVD : epitaxy, plasma assist Deposition : Metal Sputtering : Metal, insulator
Patterning	Selective deposition/etching on wafer	Photolithography Photoresist, exposure, develop Etching : Wet, Dry (plasma, ion)
Doping	Electrical property control Of wafer	Thermal diffusion Implantation

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